

REGULATOR (DDR3) 1.5VSUS, 0.75VSMDDR_VTERM,1.5V 1.5V_GPU,1.5V_CPU
REGULATOR +1.05V_VTT,+1.8V
DC/DC 3VPCU, 5VPCU, +15V PG 42
CPU Core PG 43
VGA Core Discrete PG 44

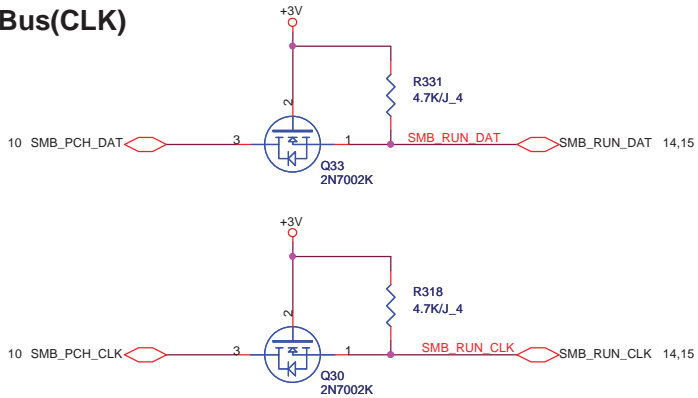
02/20 DEL for Pre-ES1


CPU_CLK select(CLK)

02/20 DEL for Pre-ES1

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus(CLK)



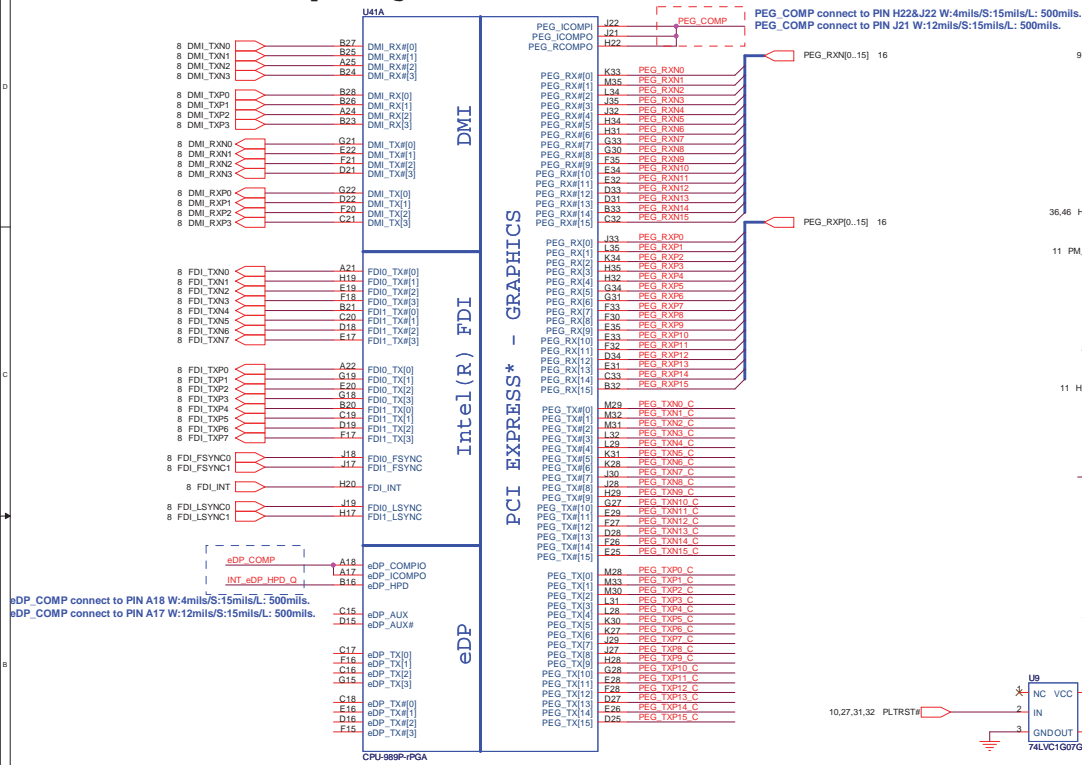


PROJECT : KL2D

Quanta Computer Inc.

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	Clock Generator	1A
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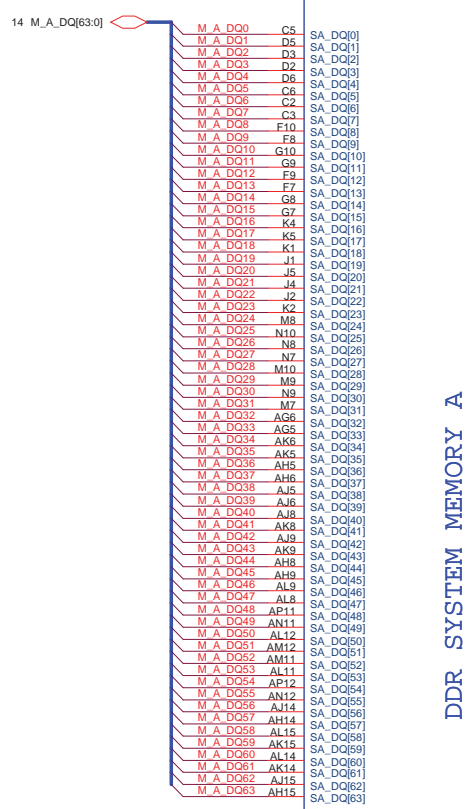
Sandy Bridge Processor (DMI,PEG,FDI)



Sandy Bridge Processor (DDR3)

05

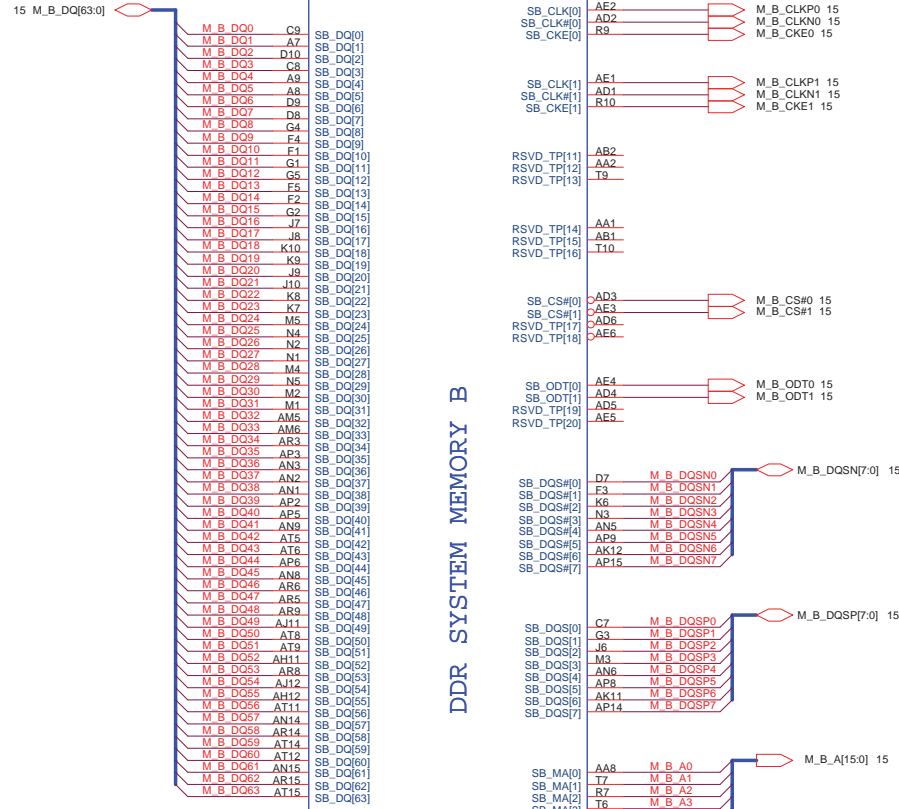
U41C



DDR SYSTEM MEMORY A

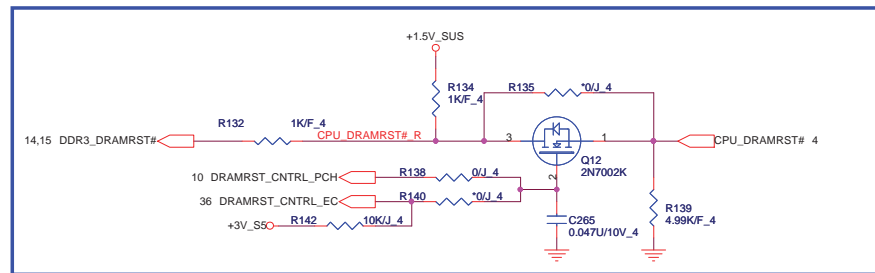
CPU-989P-1PGA

U41D



DDR SYSTEM MEMORY B

CPU-989P-1PGA

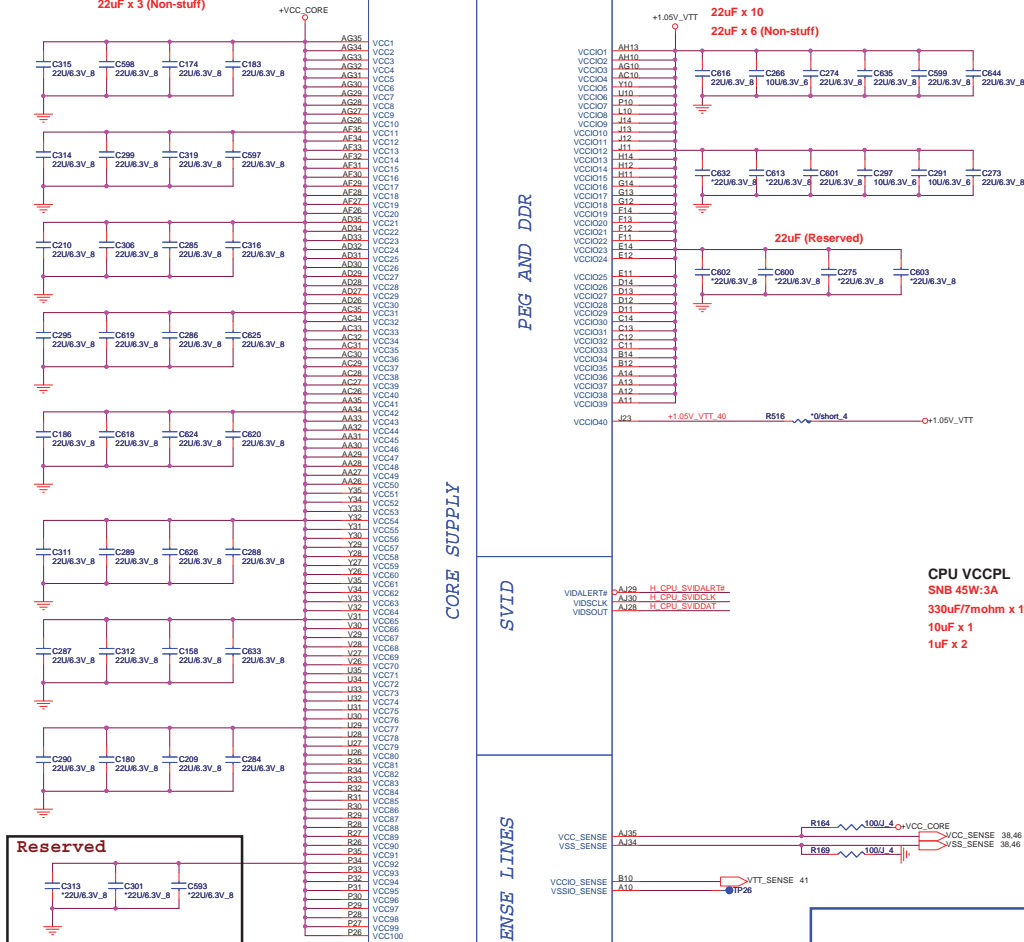


Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

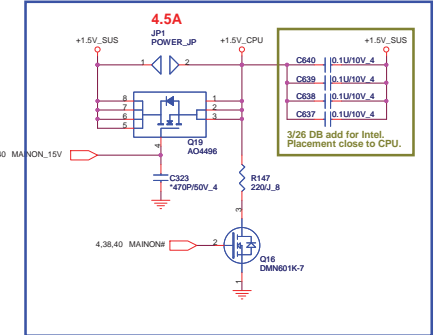
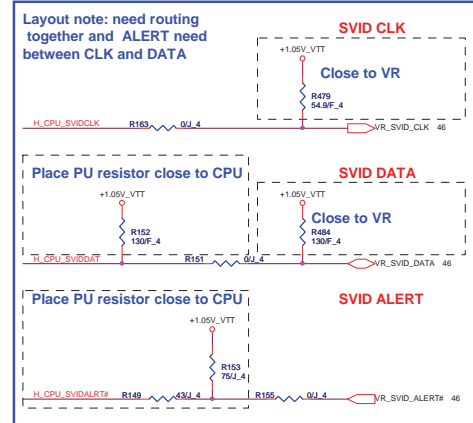
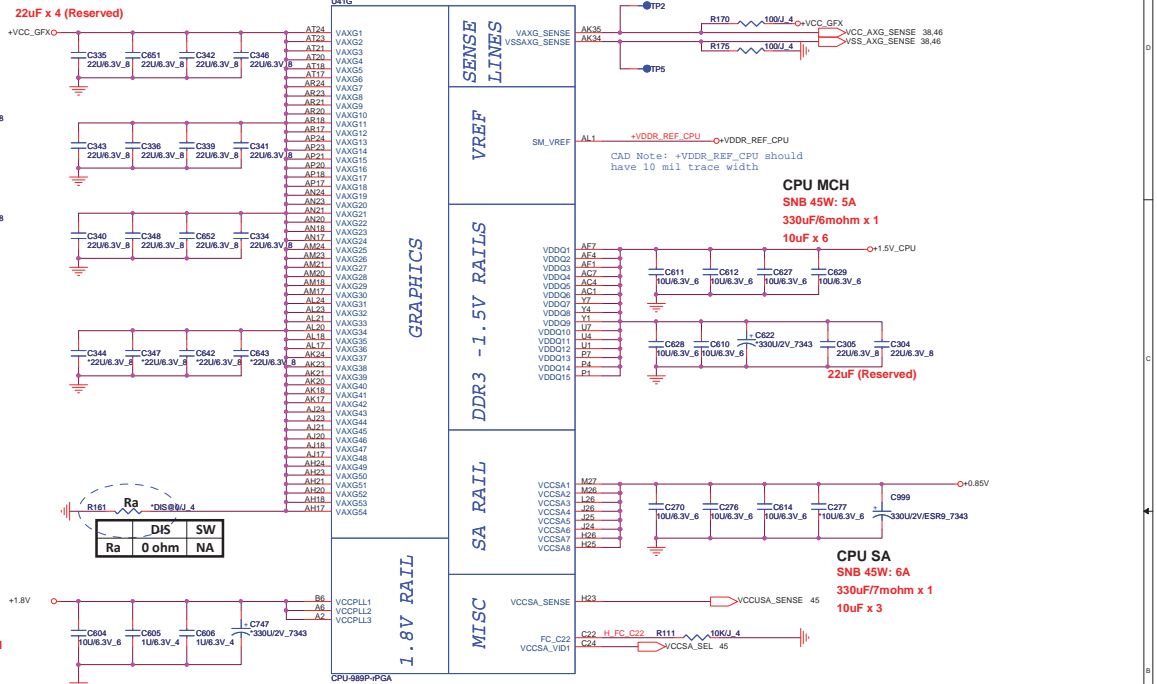
CPU Core Power
 SNB 45W:55A
 22uF x 32
 22uF x 3 (Non-stuff)

POWER



CPU VGT
 SNB 45W:22A
 22uF x 12
 22uF x 4 (Reserved)

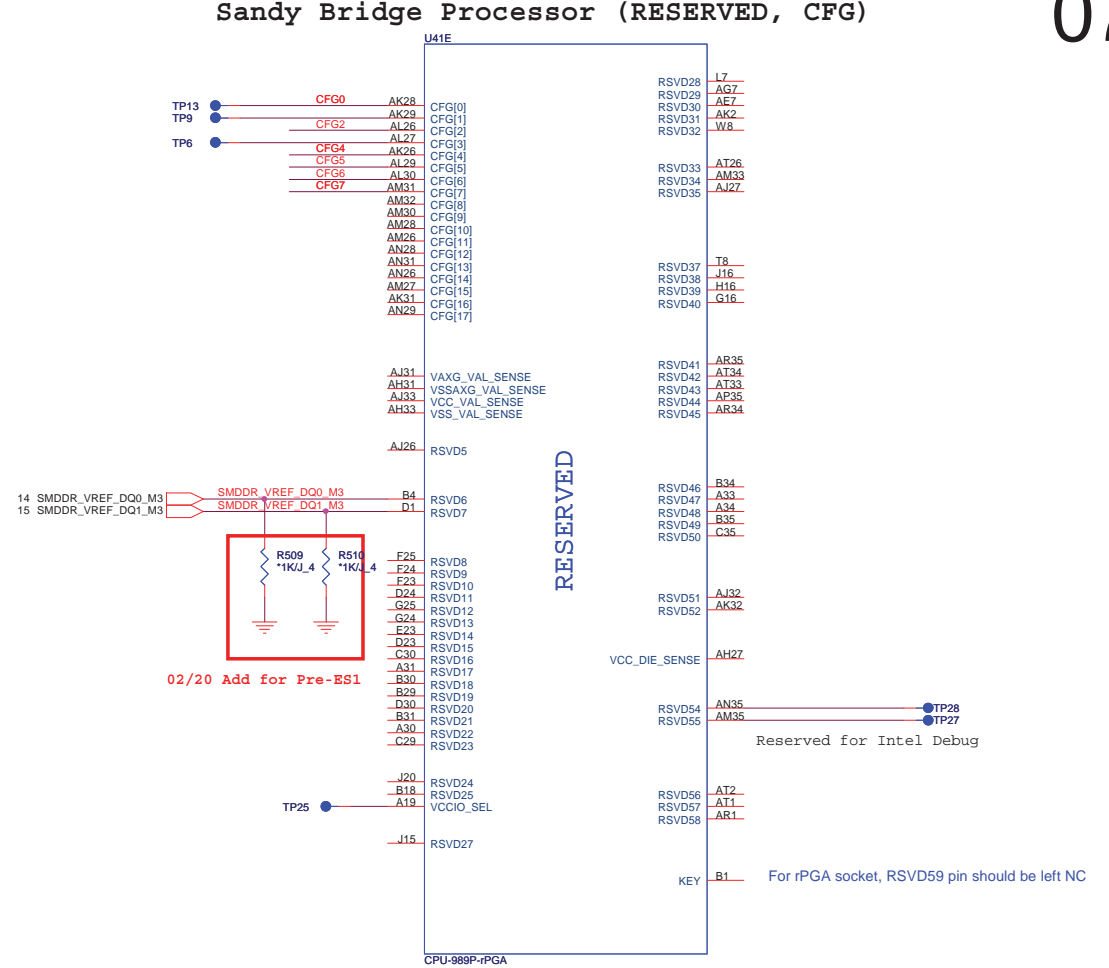
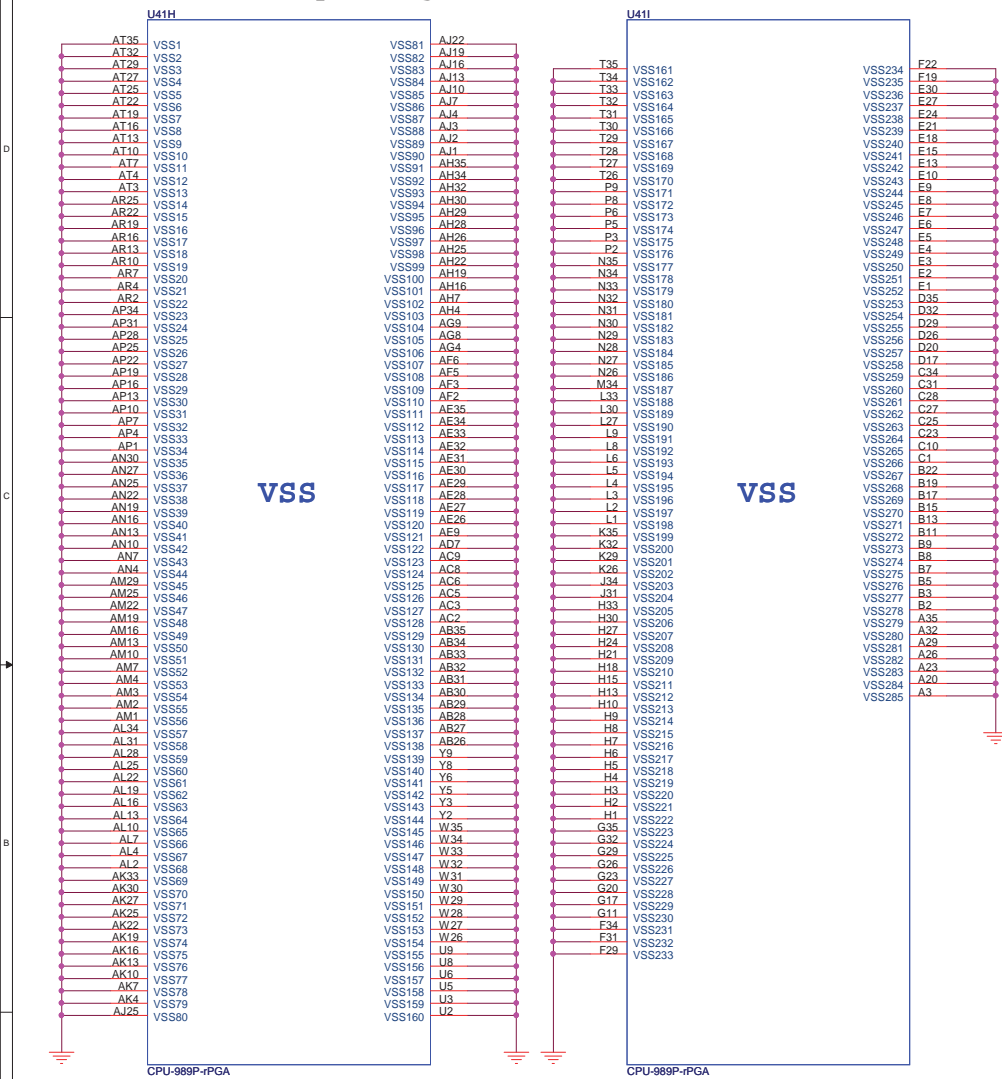
POWER



Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)

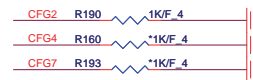
07



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)

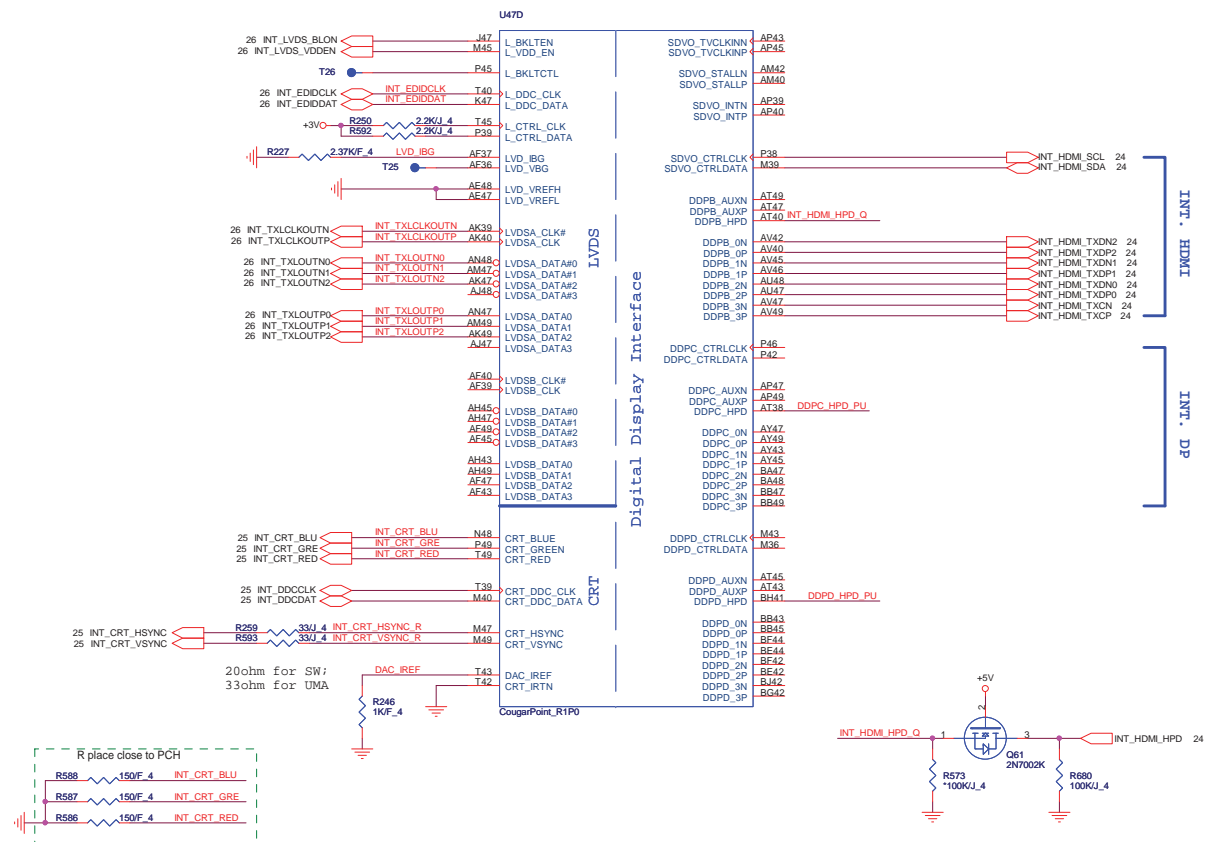
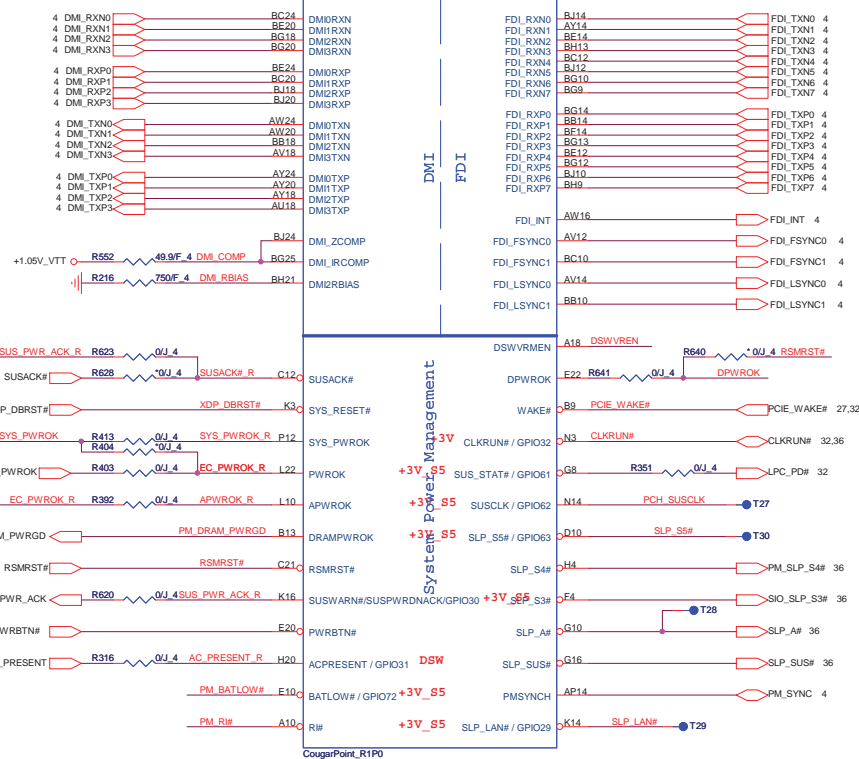
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : KL2D
Quanta Computer Inc.

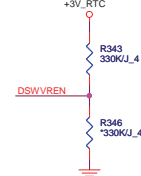
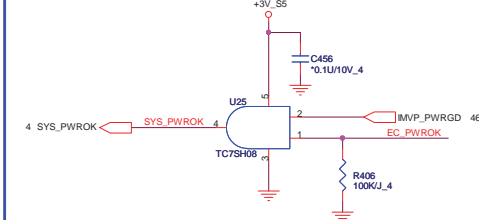
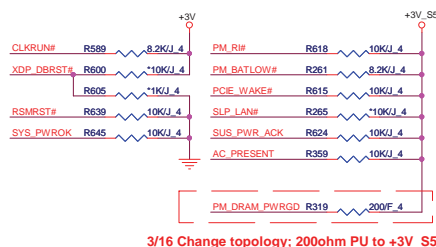
Size Document Number Rev 1A
Sandy Bridge 4/4

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U47C

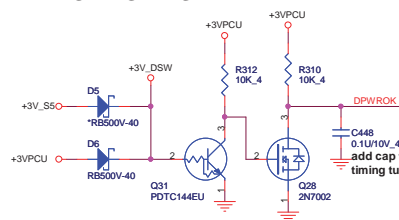


System PWR_OK(CLG)



On Die DSW VR Enable
High = Enable (Default)
Low = Disable

DPWROK FOR DSW



DDPC_HPD_PU R218 10K/J_4
DDPD_HPD_PU R559 10K/J_4

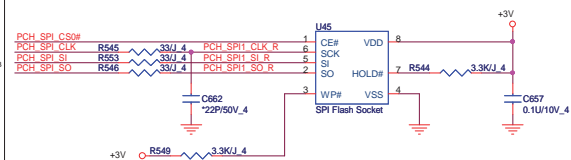
Follow PDG eDP disable guide



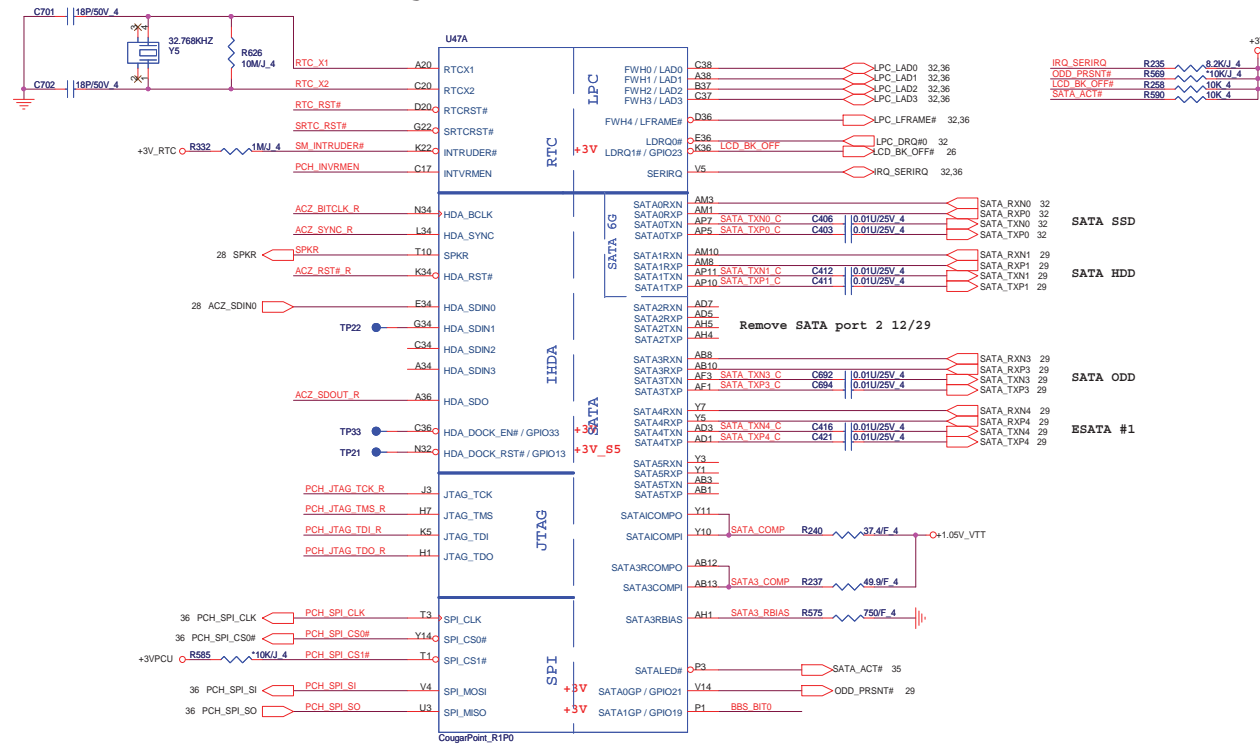
PROJECT : KL2D
Quanta Computer Inc.

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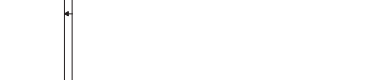
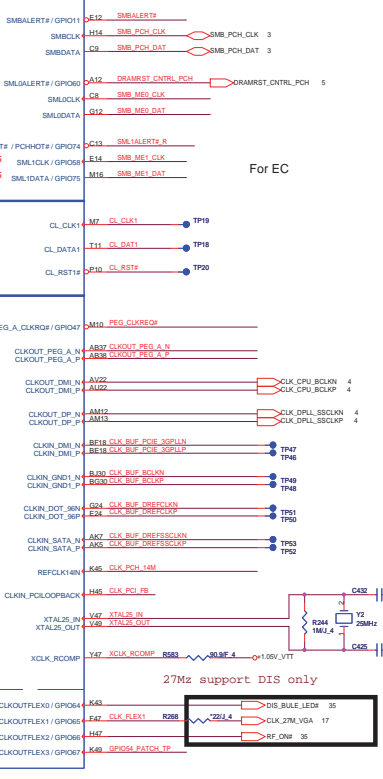
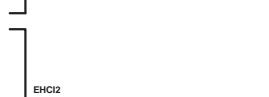
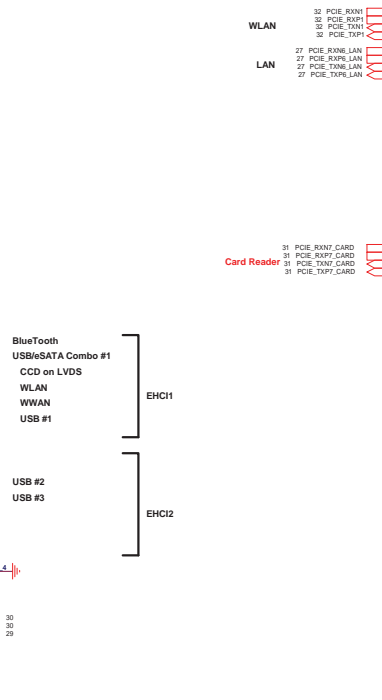
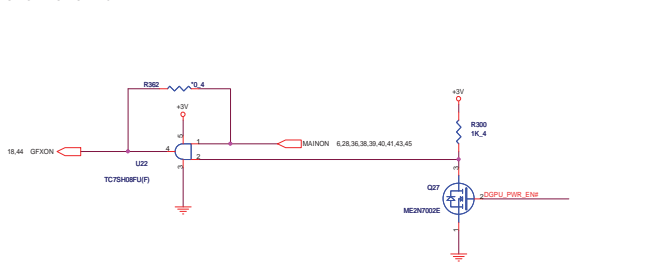
Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

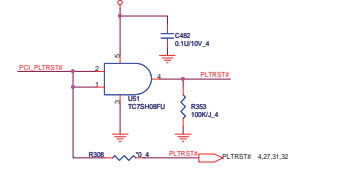
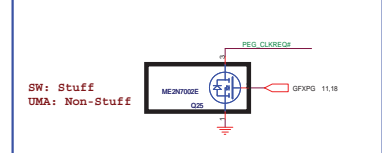
Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)										
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)										
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)										

Cougar Point-M (PCI-E, SMBUS, CLK)

[illegible]

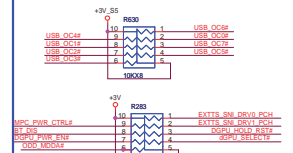
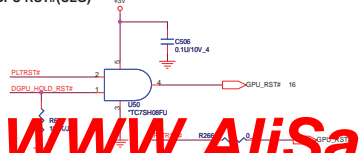
SW: Stuff
UMA: Non-Stuff

Timing diagram is not to scale



Pin connections for the USB module:

- RE30 Connector:**
 - Pin 1: USB_OCMF
 - Pin 2: USB_O0M
 - Pin 3: USB_OCMF
 - Pin 4: USB_OCMF
 - Pin 5: USB_OCMF
 - Pin 6: USB_OCMF
 - Pin 7: USB_OCMF
 - Pin 8: USB_OCMF
- R28B Connector:**
 - Pin 1: EXTFS_SIN_DRV1_PCH
 - Pin 2: EXTFS_SIN_DRV1_PCH
 - Pin 3: EXTFS_SIN_DRV1_PCH
 - Pin 4: EXTFS_HOLD_RSTFS
 - Pin 5: EXTFS_HOLD_RSTFS

[illegible]

LAN

- 32 CLK_PCIE_WLAN → R258 → CLKOUT_P0P0N → P0CIECLKP0P0
- 33 CLK_PCIE_LAN0 → R259 → CLKOUT_P0P0N → P0CIECLKP0P0
- 34 CLK_PCIE_LAN1 → R260 → CLKOUT_P0P0N → P0CIECLKP0P0
- 37 CLK_PCIE_LAN2 → R261 → CLKOUT_P0P0N → P0CIECLKP0P0

Card Reader

- 31 CLK_PCIE_CAD0 → R262 → CLKOUT_P0P0N → P0CIECLKP0P0
- 32 CLK_PCIE_CAD1 → R263 → CLKOUT_P0P0N → P0CIECLKP0P0
- 33 CLK_PCIE_CAD2 → R264 → CLKOUT_P0P0N → P0CIECLKP0P0
- 34 CLK_PCIE_CAD3 → R265 → CLKOUT_P0P0N → P0CIECLKP0P0

SW:Stuff

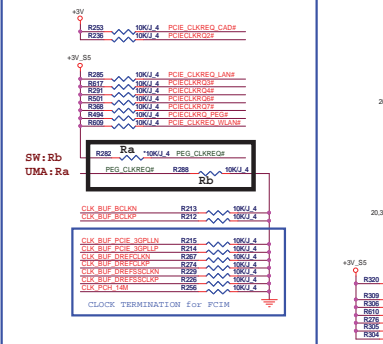
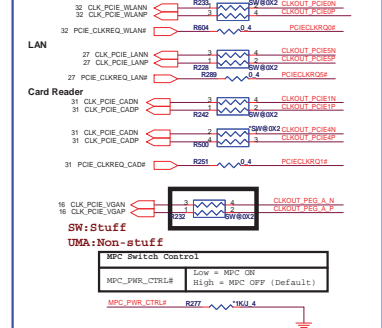
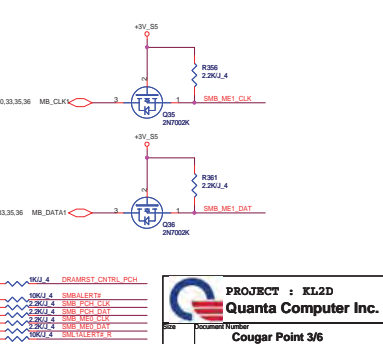
16 CLK_PCIE_VIOA → SW9061 → CLKOUT_P0P0N → P0CIECLKP0P0

17 CLK_PCIE_VIOAP → SW9061 → CLKOUT_P0P0N → P0CIECLKP0P0

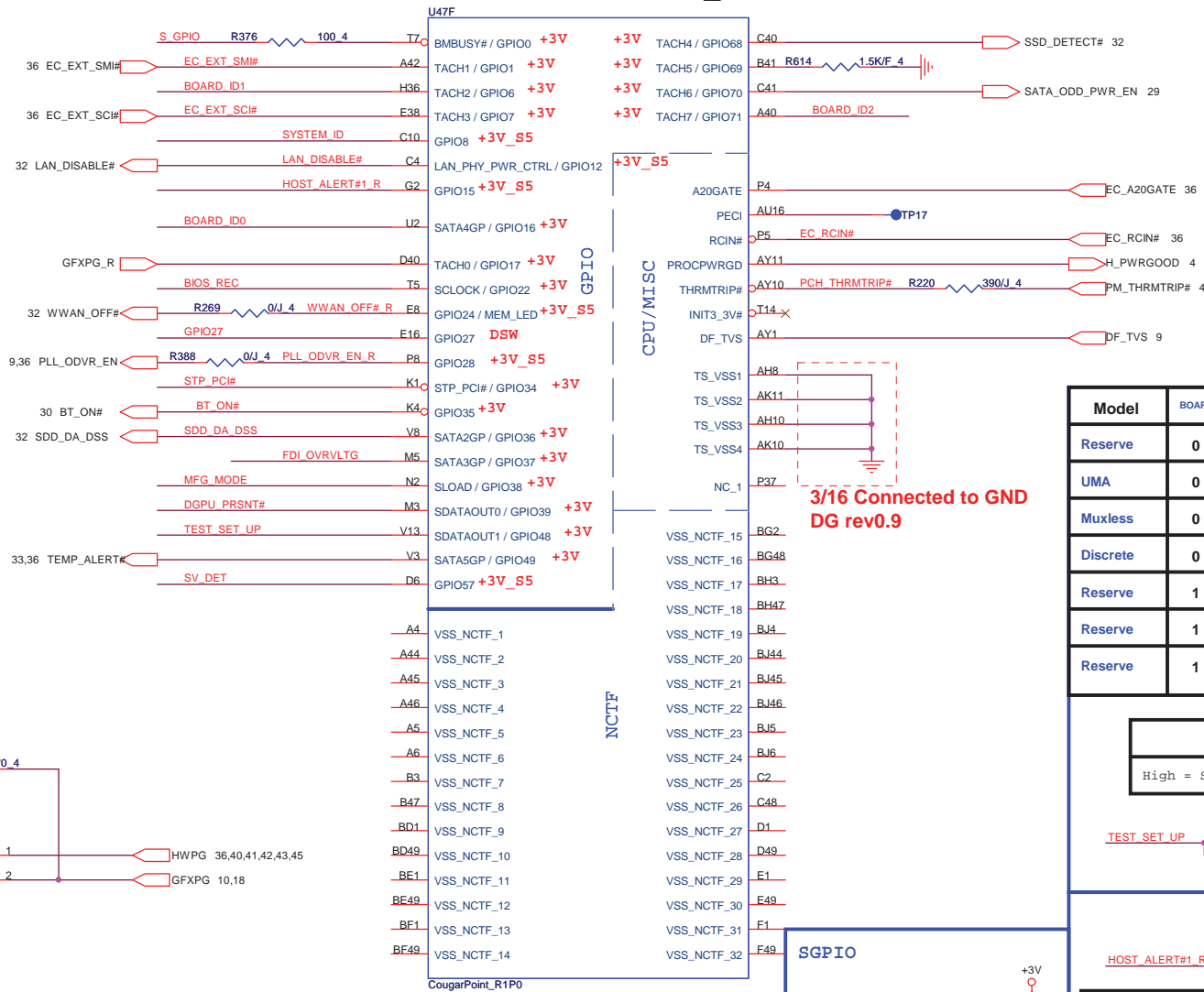
MPC Switch Control

MPC_SW_CTRL0	Low = MPC_ON
MPC_SW_CTRL1	High = MPC_OFF (Default)

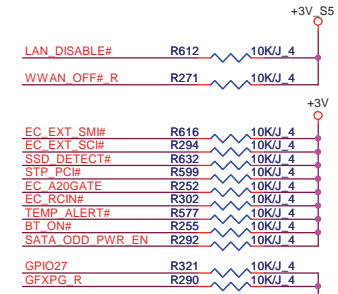
MPC_PWR_CTRL0 → R277 → R278 → 0.4

[illegible]

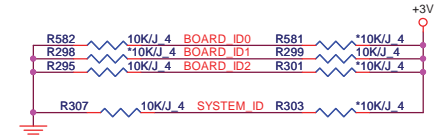
Cougar Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down(CLG)



Model	BOARD_ID2	BOARD_ID1	BOARD_ID0
Reserve	0	0	0
UMA	0	0	1
Muxless	0	1	0
Discrete	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0



SV_SET_UP

High = Strong (Default)



HOST_ALERT#1_R R607 1K/J 4

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

MFG-TEST

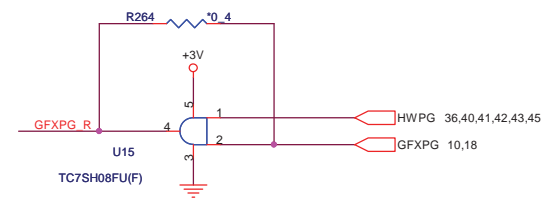


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Quanta Computer Inc.

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FDI TERMINATION VOLTAGE OVERRIDE

LOW - Tx, Rx terminated to same voltage

DMI TERMINATION VOLTAGE OVERRIDE

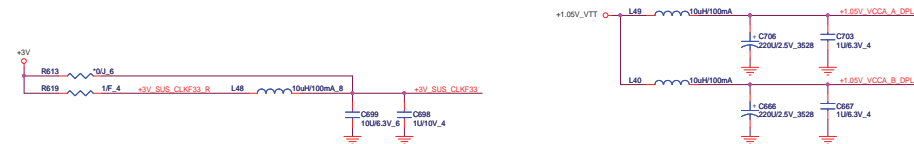
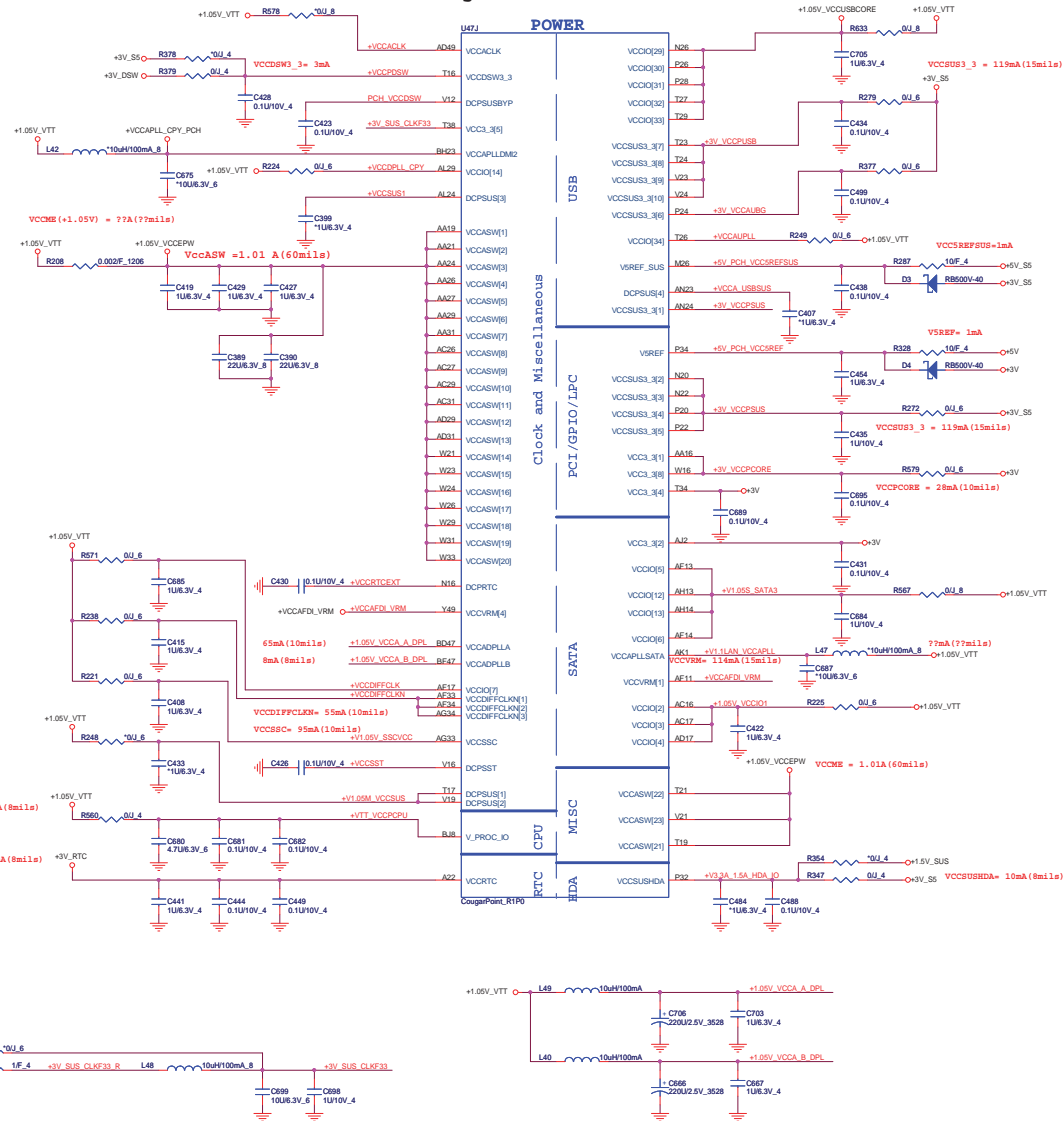
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS RECOVERY

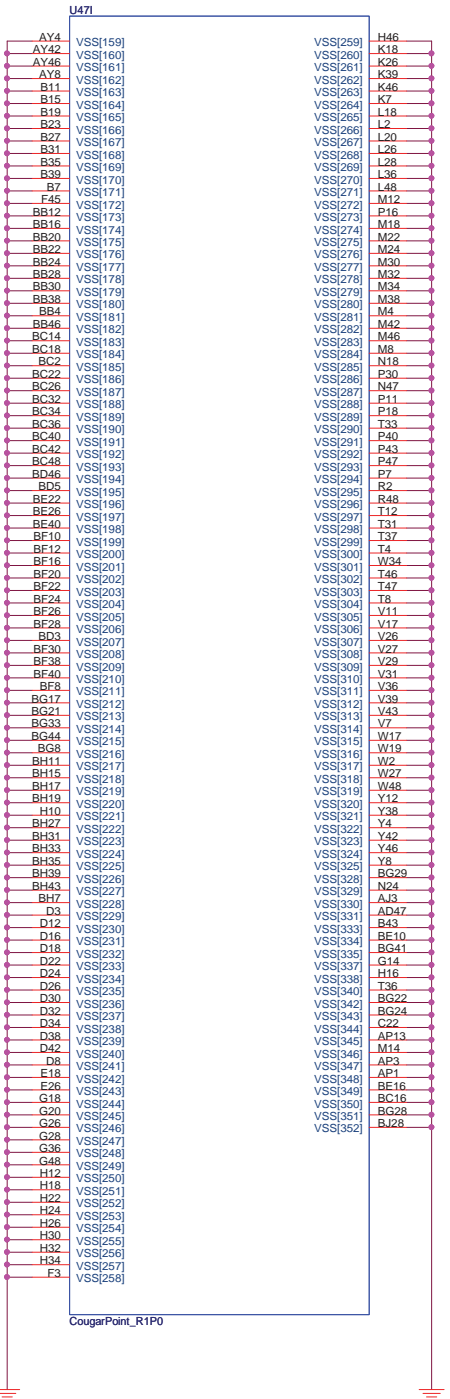
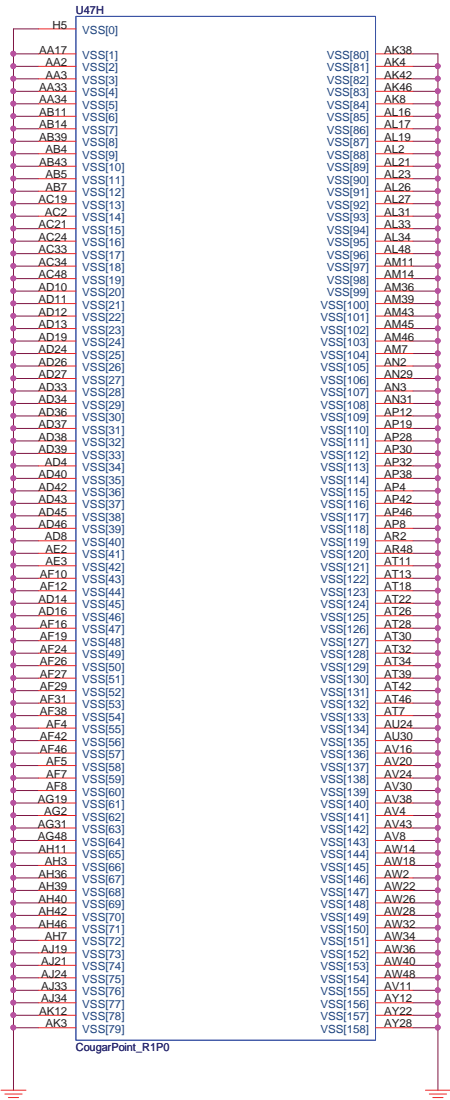
High = Disable (Default)

Low = Enable

Cougar Point-M (POWER)

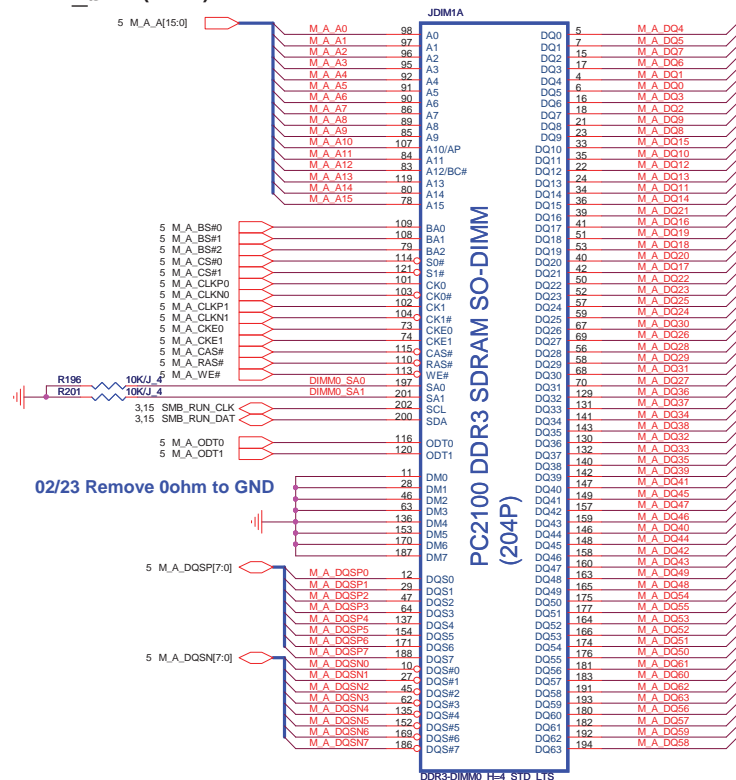


IBEX PEAK-M (GND)

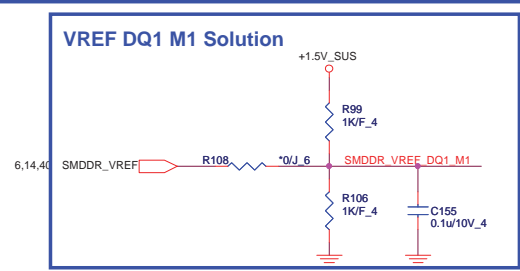
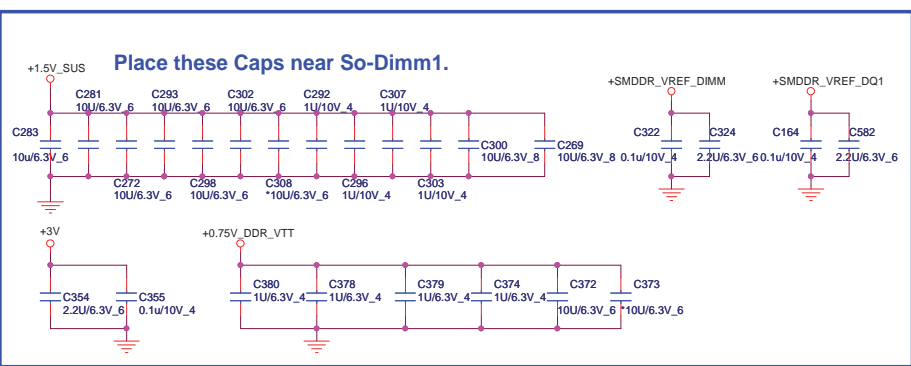
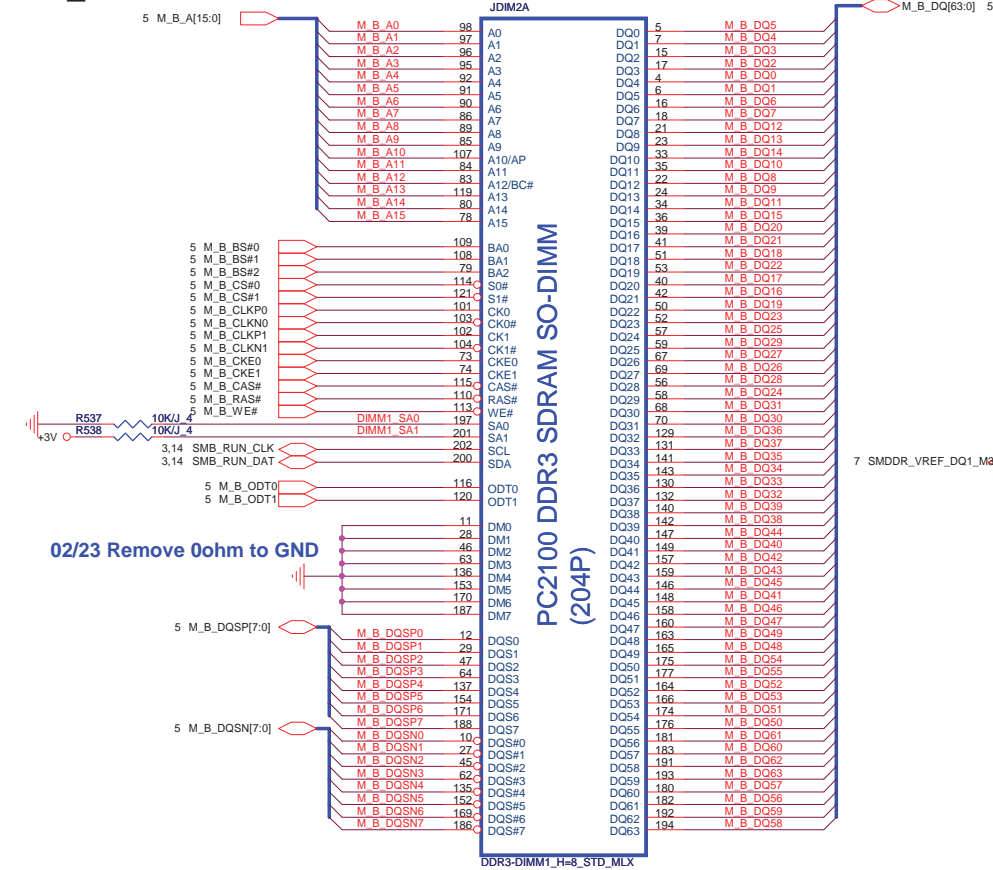


DDR_STD (DDR)

14

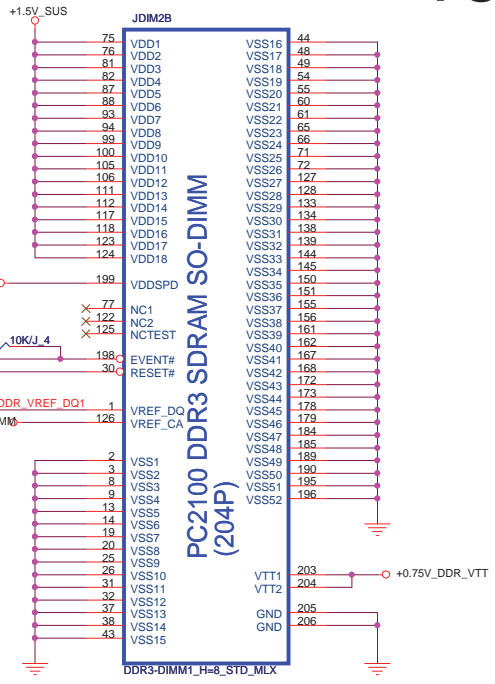
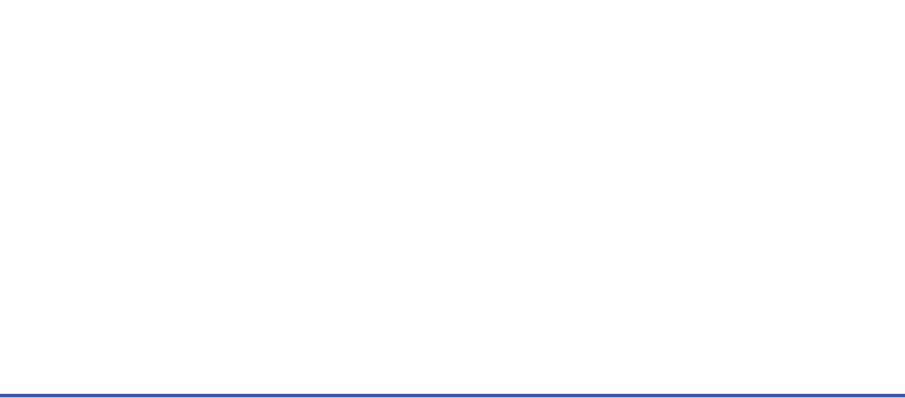


DDR_RVS (DDR)



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		

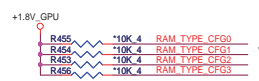
VREF DQ1 M2 Solution



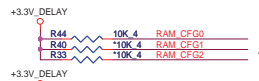


Memory Straps		RAM TYPE_CFG3	RAM TYPE_CFG2	RAM TYPE_CFG1	RAM TYPE_CFG0
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	0	0	0	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	0	0	0	1
		0	0	1	0
		0	1	0	0
		0	1	0	1

Note : Required Frequency = 800 MHz



VRAM TYPE



APERTURE SIZE

MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

Access to SCL and SDA is mandatory on BACQ design for debug purposes.

NC FOR PARK

NC FOR PARK

+3.3V_DELAY

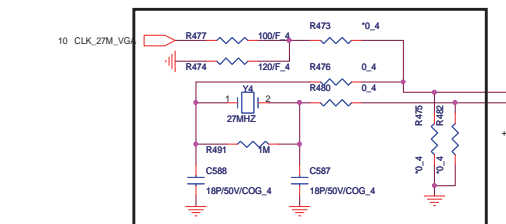
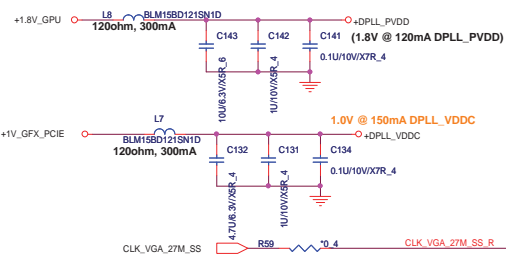
*4.7K_4

*4.7K_4



GPU Power-on sequence

- 1 => +VGPU_CORE
- 2 => +VGPU_IO
- 3 => +1V
- 4 => +1.5V_GPU
- 5 => +3V_D
- 6 => +1.8V_GPU
- 7 => dGPU_PWROK



Use 27MHz Crystal for A test Danny0518

Power PWM config

EXT_PANEL_BKEN

GPIO0 AH20

GPIO1 AH18

GPIO2 AH16

GPIO3 AH23

GPIO4 AH23

GPIO5 AH17

GPIO6 AH17

GPIO7 AH13

GPIO8 AH15

GPIO9 AH16

GPIO10 AH16

GPIO11 AH16

GPIO12 AH16

GPIO13 AH14

GPIO14 AH14

GPIO15 AH14

GPIO16 AH14

GPIO17 AH14

GPIO18 AH14

GPIO19 AH14

GPIO20 AH14

GPIO21 AH14

GPIO22 AH14

GPIO23 AH14

GPIO24 AH14

GPIO25 AH14

GPIO26 AH14

GPIO27 AH14

GPIO28 AH14

GPIO29 AH14

GPIO30 AH14

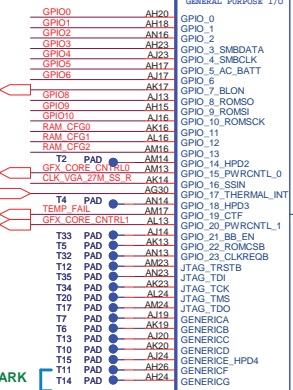
GPIO31 AH14

GPIO32 AH14

GPIO33 AH14

GPIO34 AH14

GPIO35 AH14



GenericF/G is NC on PARK

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

EXT_HDMI_HPD

1.8V_GPU

499F_4

1.8V @ 120mA DPLL_VDDC

0.1u/10V/X7R_4

1.0V @ 150mA DPLL_VDDC

0.1u/10V/X7R_4

1.8V @ 120mA DPLL_VDDC

0.1u/10V/X7R_4

1.8V @ 120mA DPLL_VDDC

0.1u/10V/X7R_4

1.8V @ 120mA DPLL_VDDC

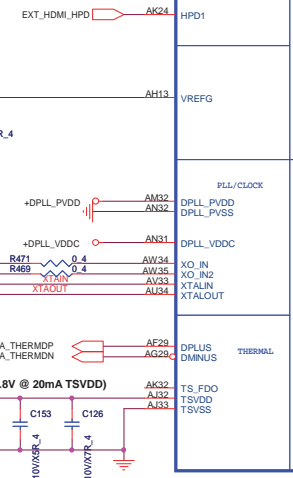
0.1u/10V/X7R_4

1.8V @ 120mA DPLL_VDDC

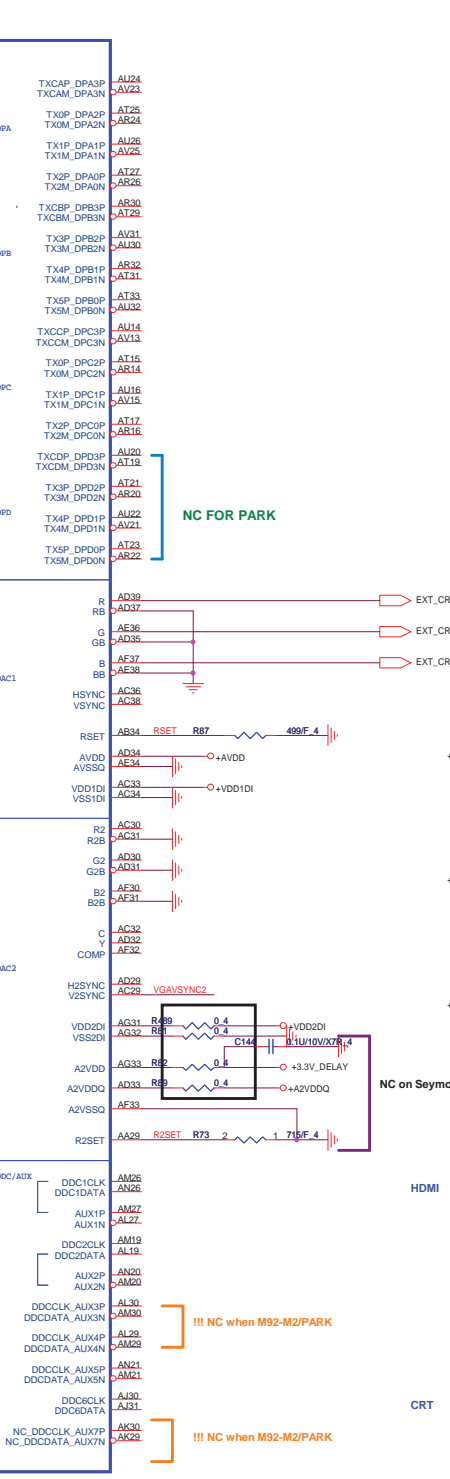
0.1u/10V/X7R_4

1.8V @ 120mA DPLL_VDDC

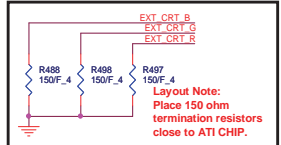
0.1u/10V/X7R_4



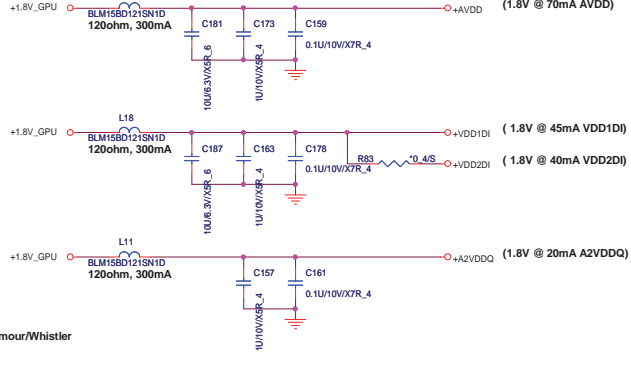
Capilano Pro/Robson_M2



CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	1
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0



Layout Note: Place 150 ohm termination resistors close to ATI CHIP.



HDMI

CRT

!!! NC when M92-M2/PARK

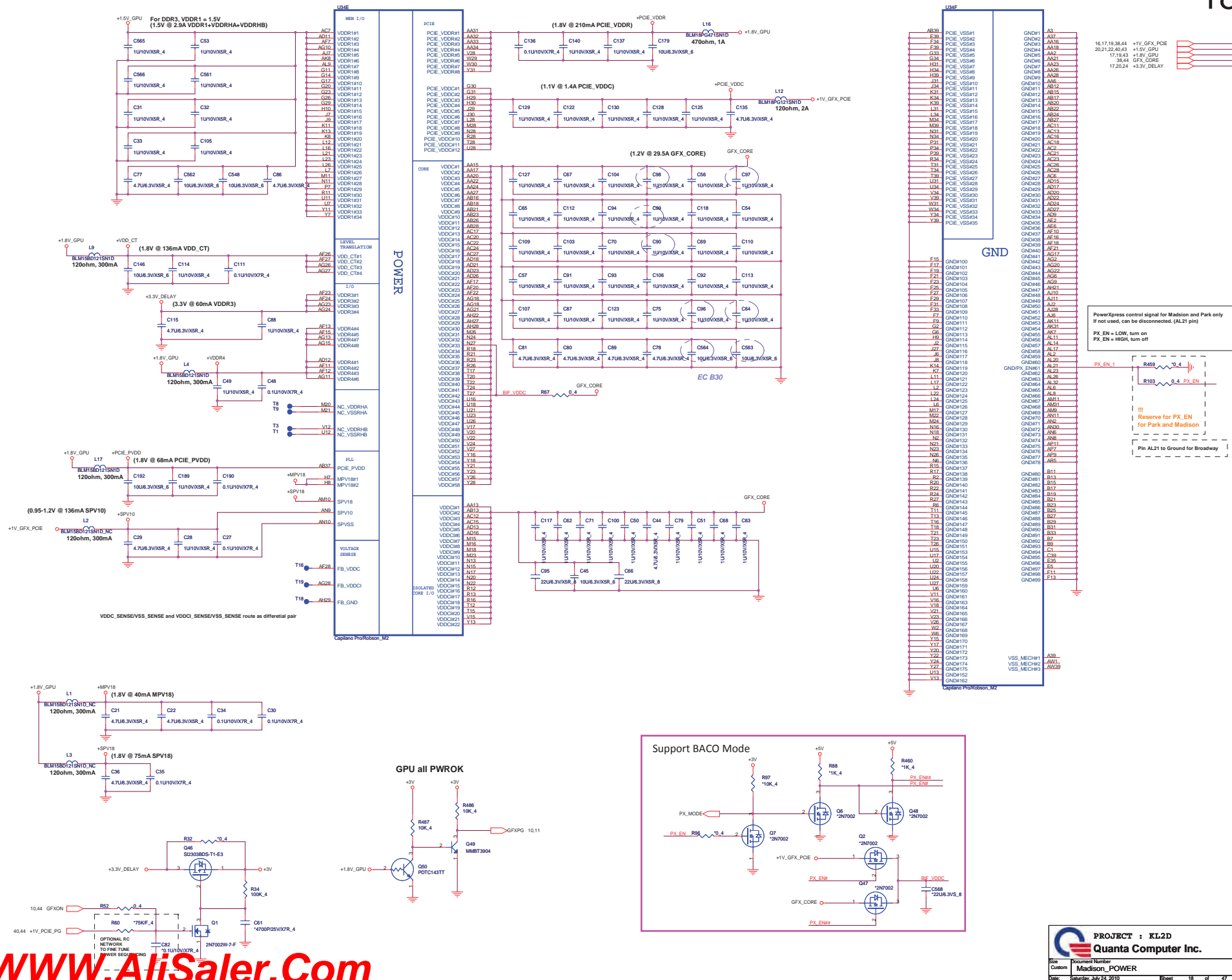
!!! NC when M92-M2/PARK

DDC6CLK/DDC6DATA support internal HDCP(High-bandwidth Digital Content Protection) function.



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Quanta Computer Inc.

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	Madison_IO&STRAP	
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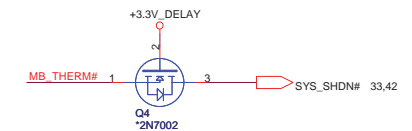




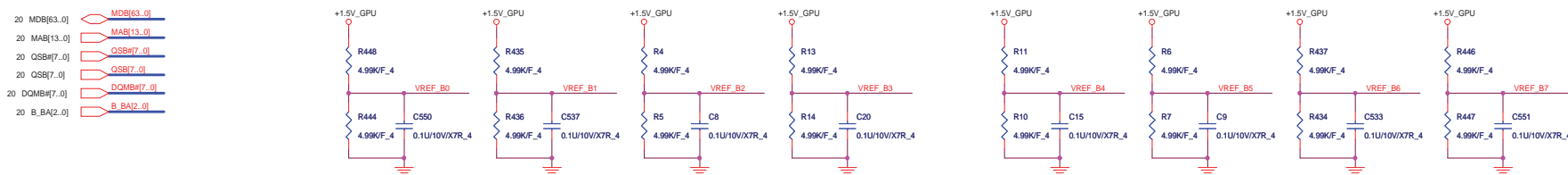
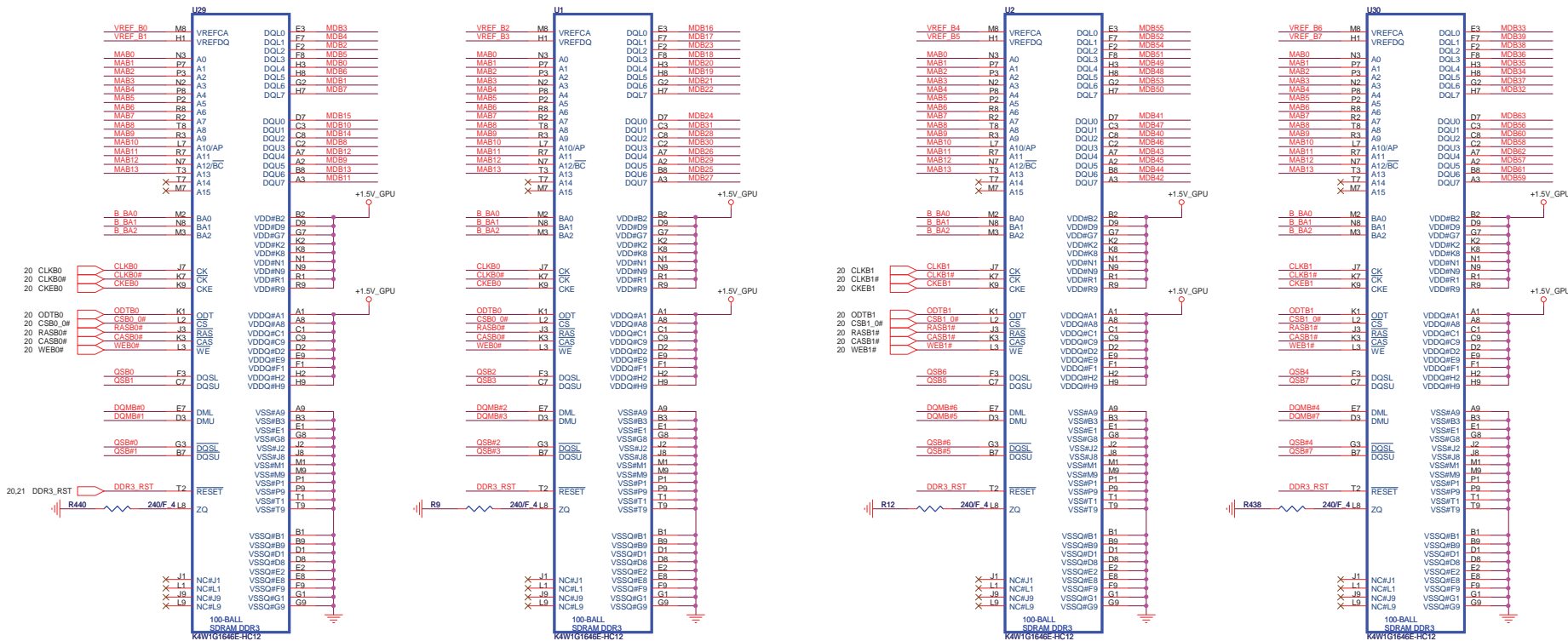


DDR3/GDDR3 Memory Stuff Option

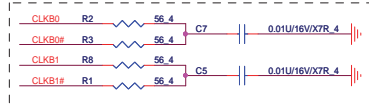
	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	100R
Rb	100R	100R







Placement has to be close to VRAM

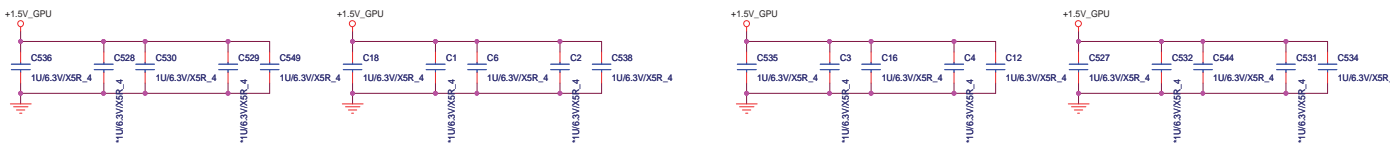


Close to U35

Close to U1

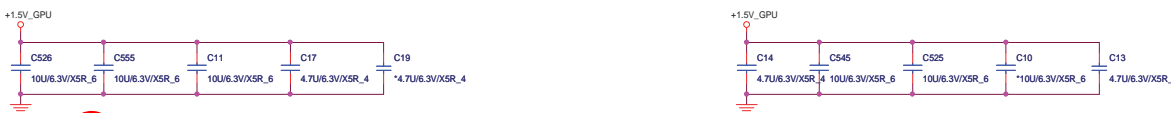
Close to U2

Close to U36

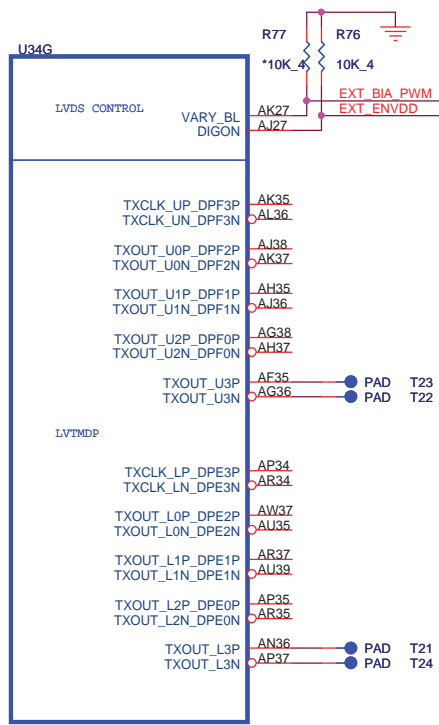


Close to U35 & U1

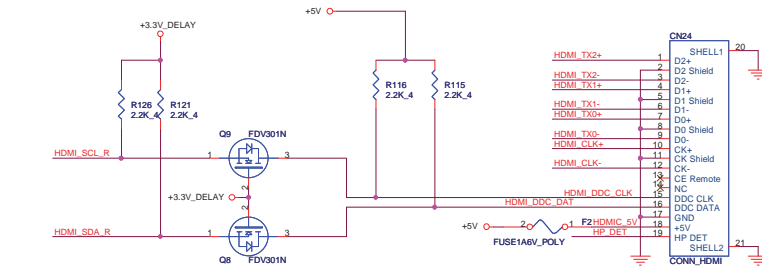
Close to U2 & U36



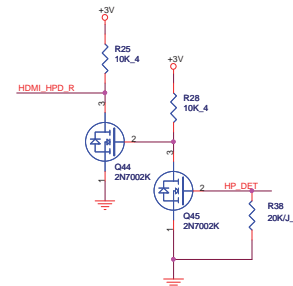
CRT SWITCH



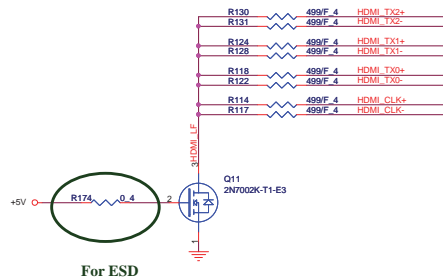
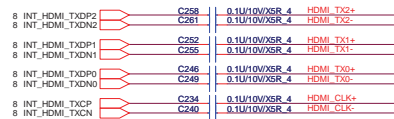
Capilano Pro/Robson_M2



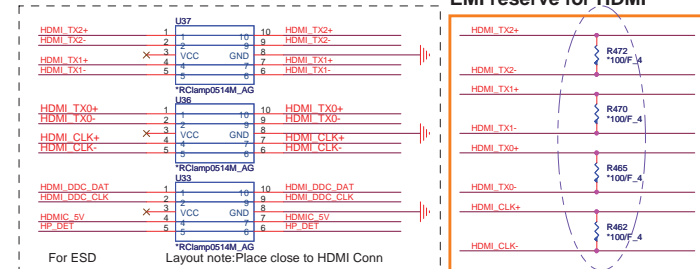
HDMI Hot-PLUG to EC and GPU

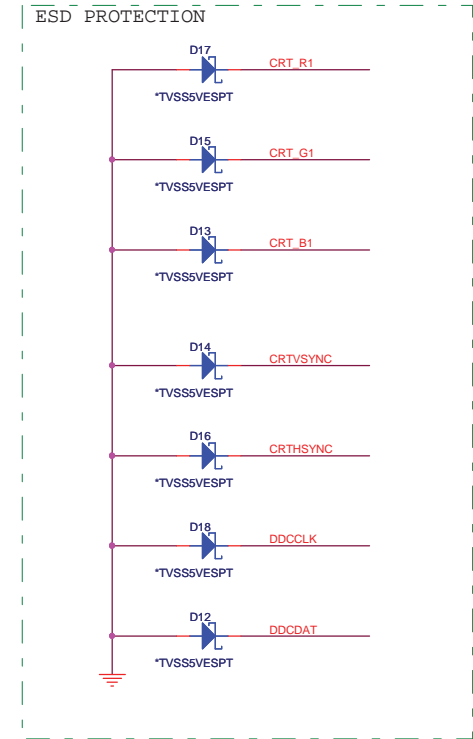
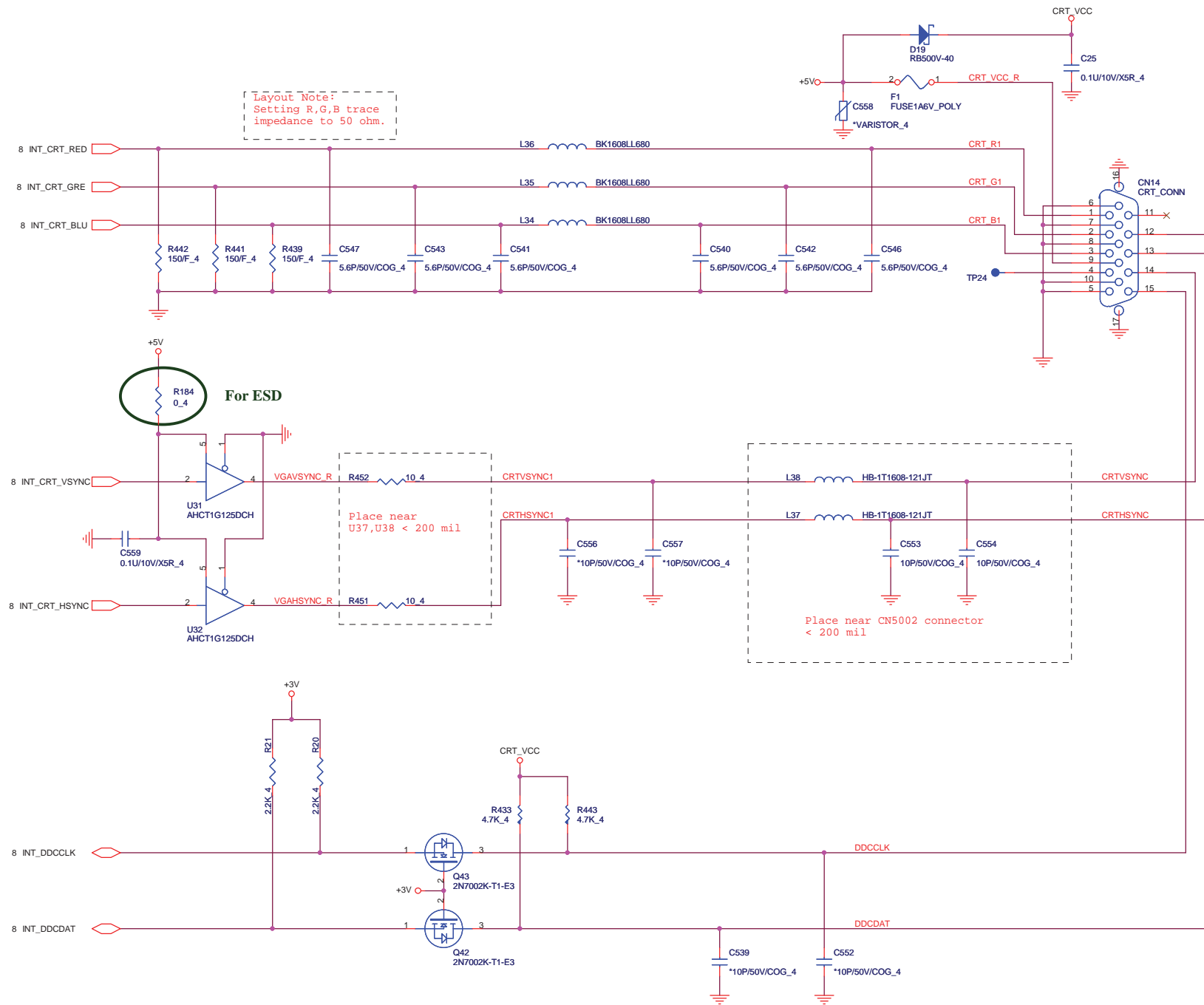


UMA Only / Muxless HDMI

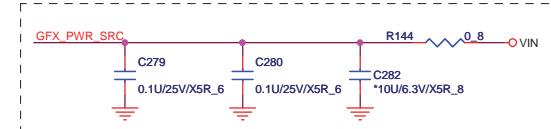
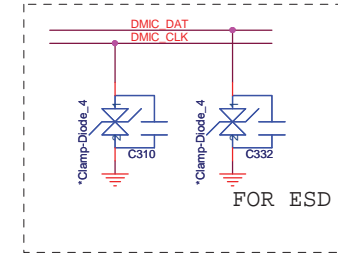
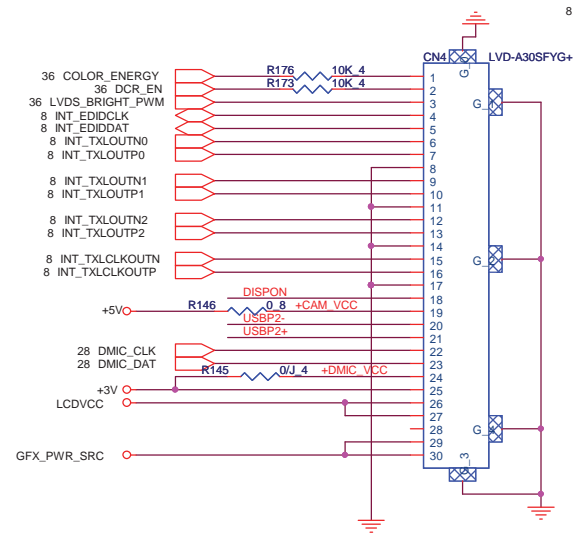
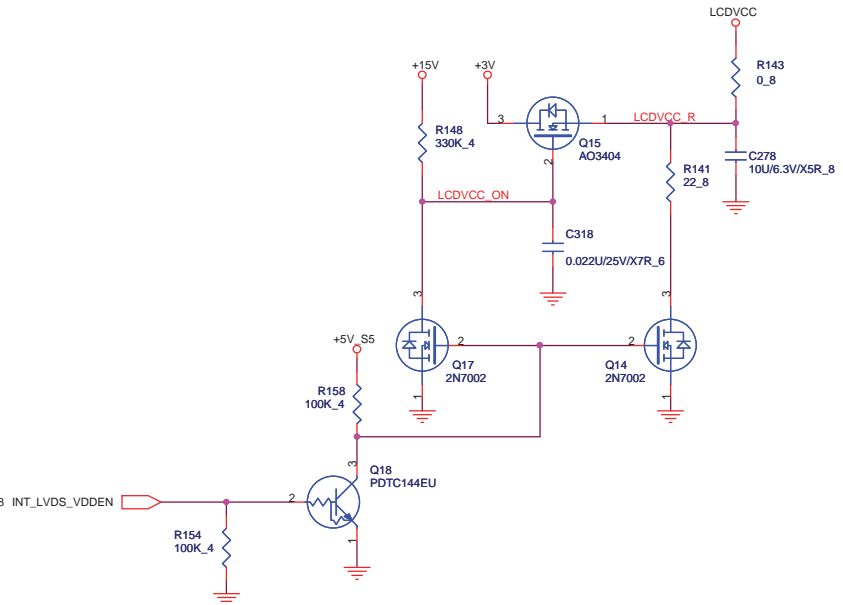


EMI reserve for HDMI

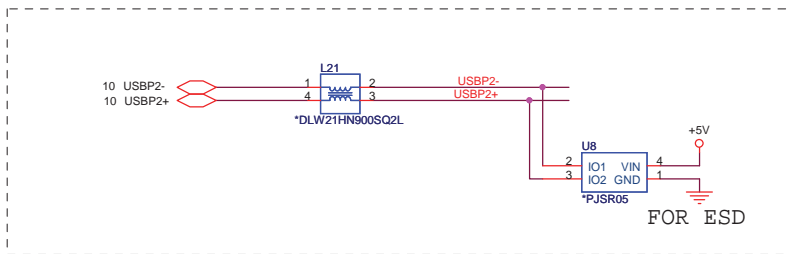
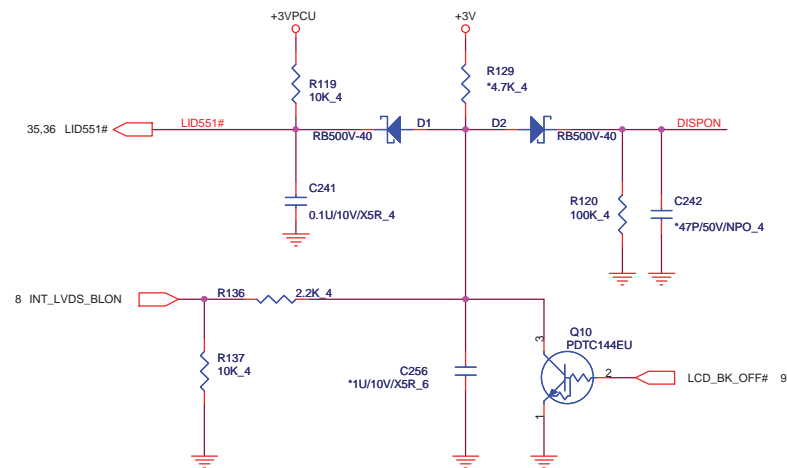





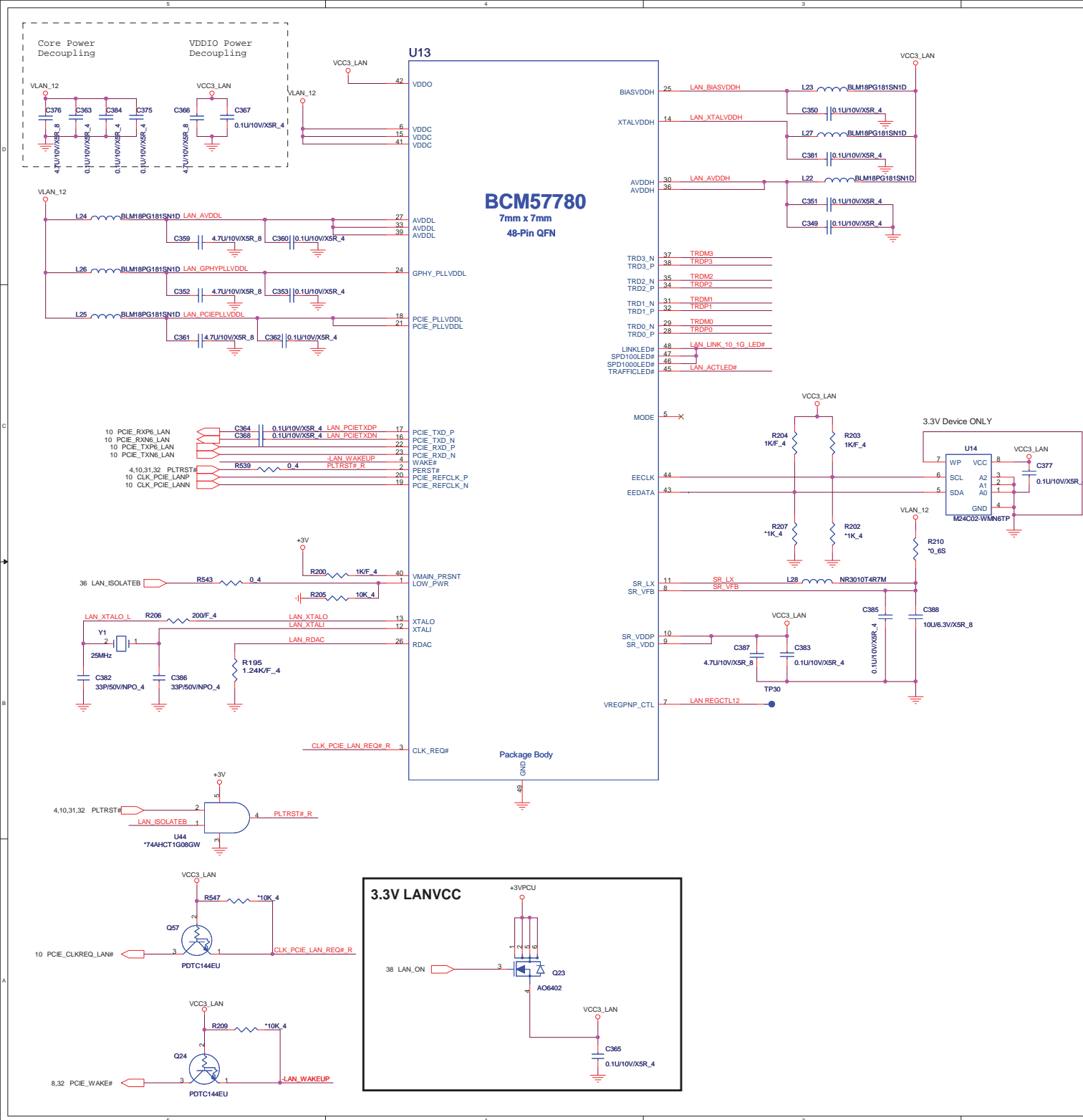
LCDVCC



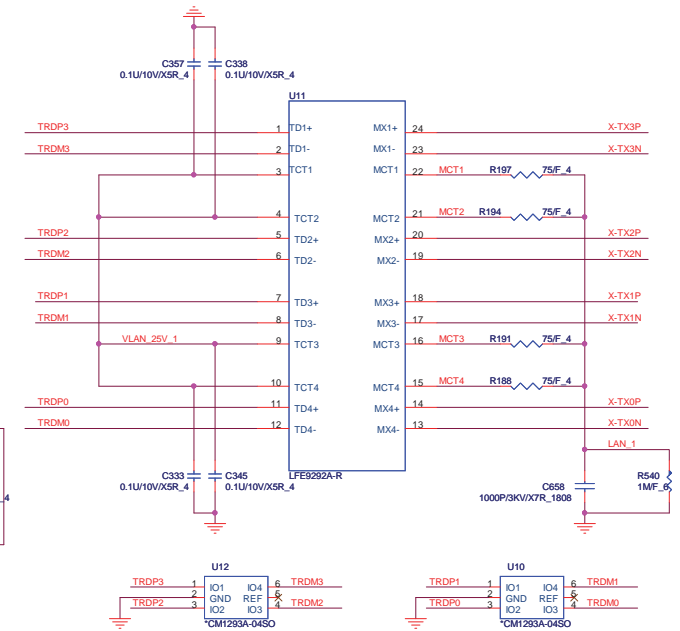
back light



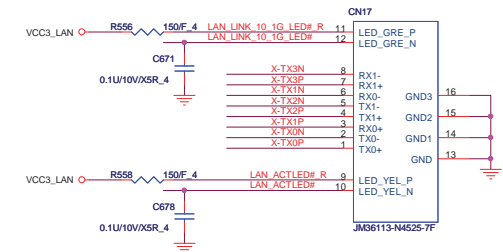
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	Quanta Computer Inc.		
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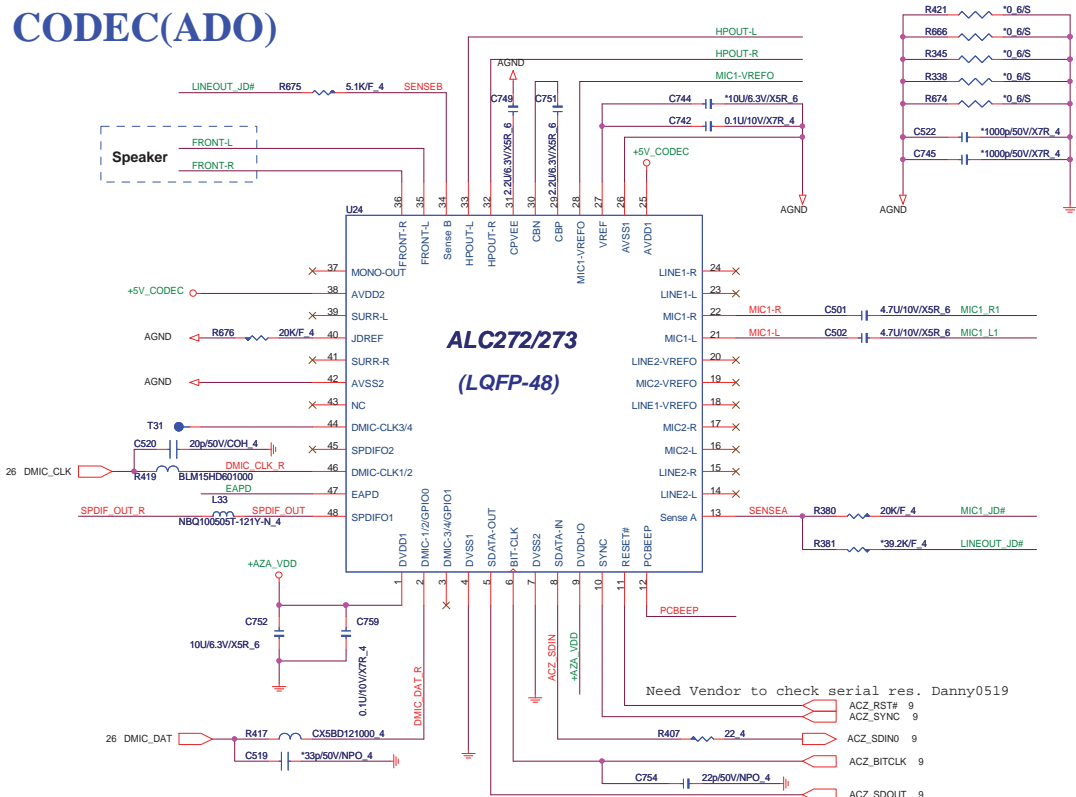
Transformer



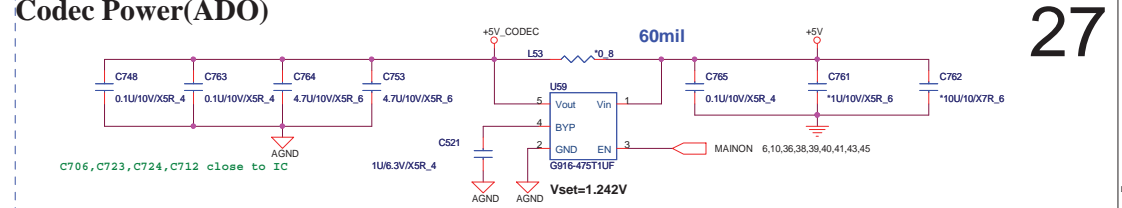
RJ45 Connector



CODEC(ADO)

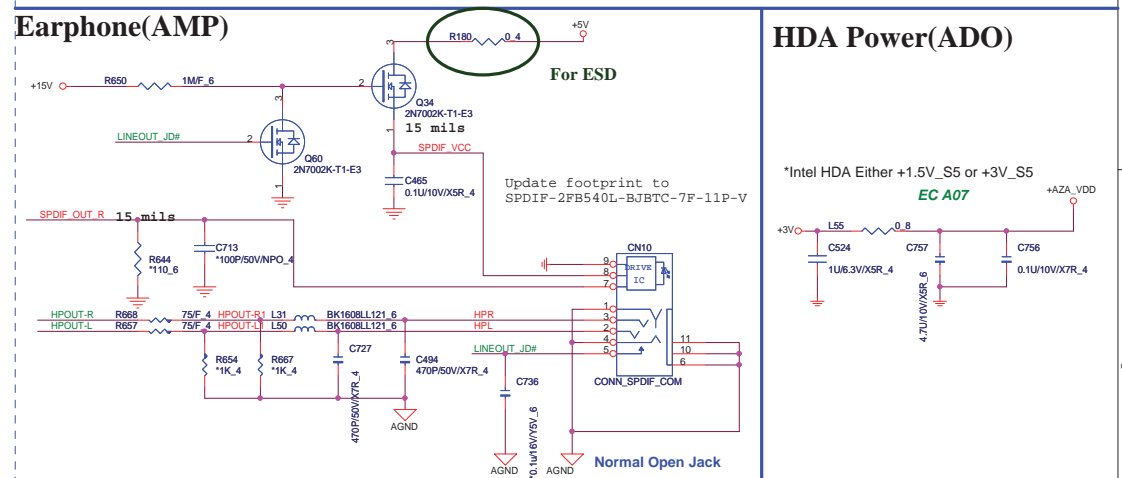


Codec Power(ADO)

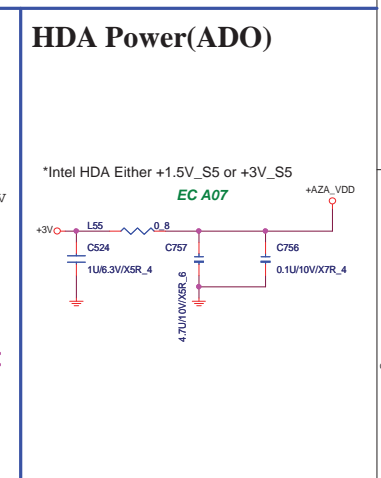


27

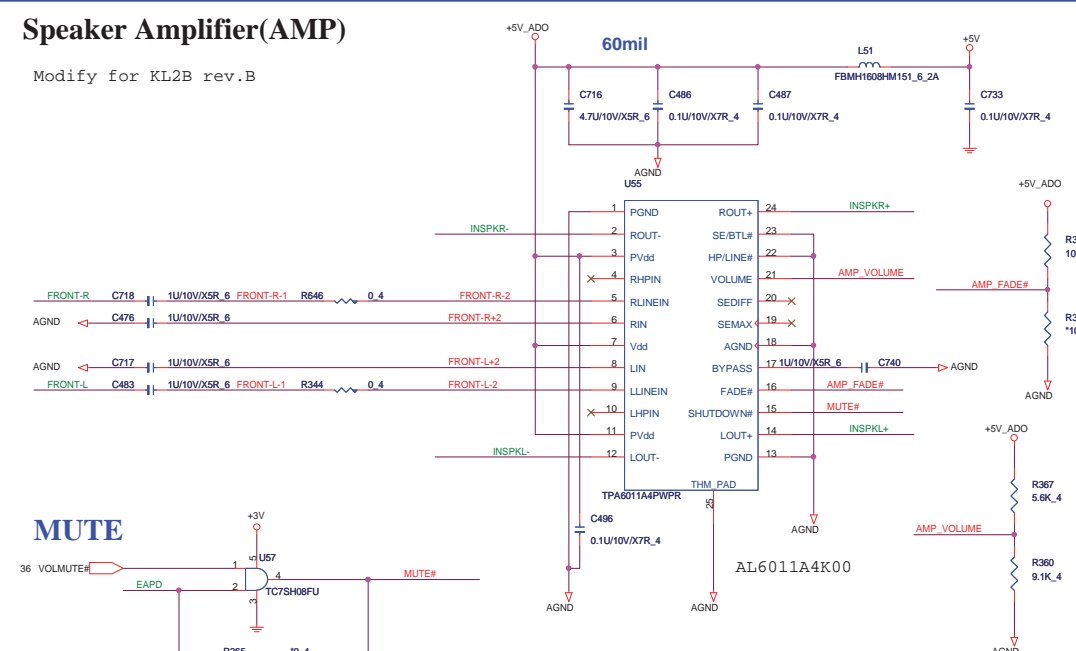
Earphone(AMP)



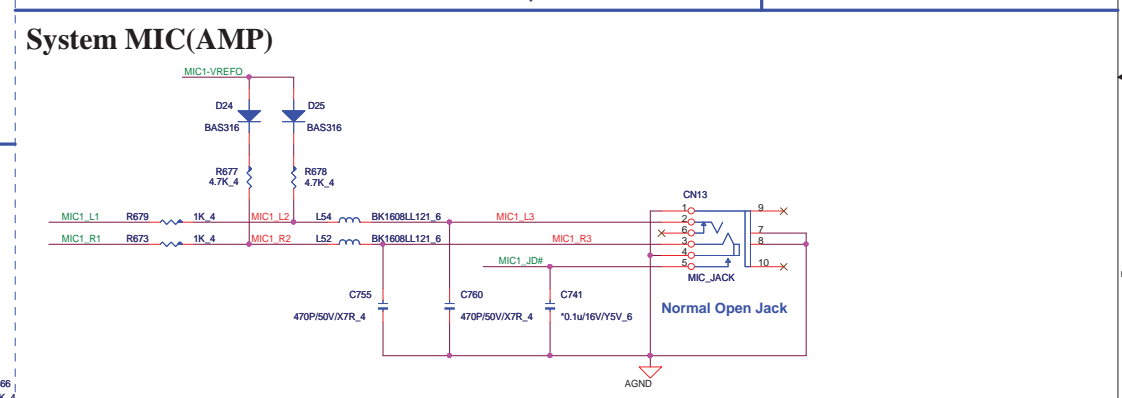
HDA Power(ADO)



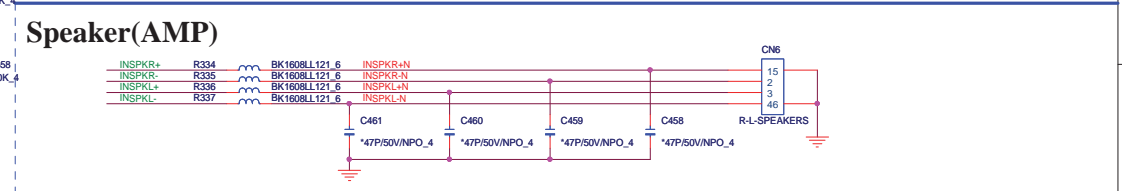
Speaker Amplifier(AMP)



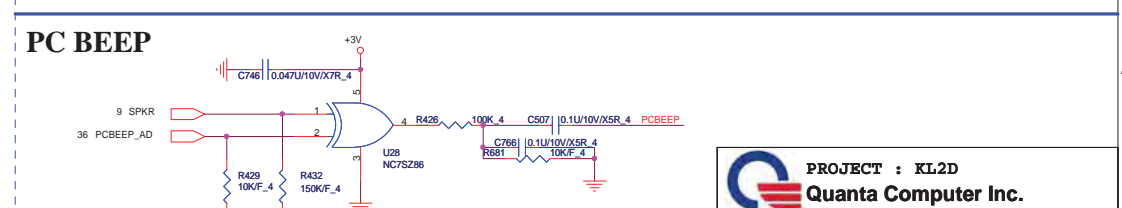
System MIC(AMP)



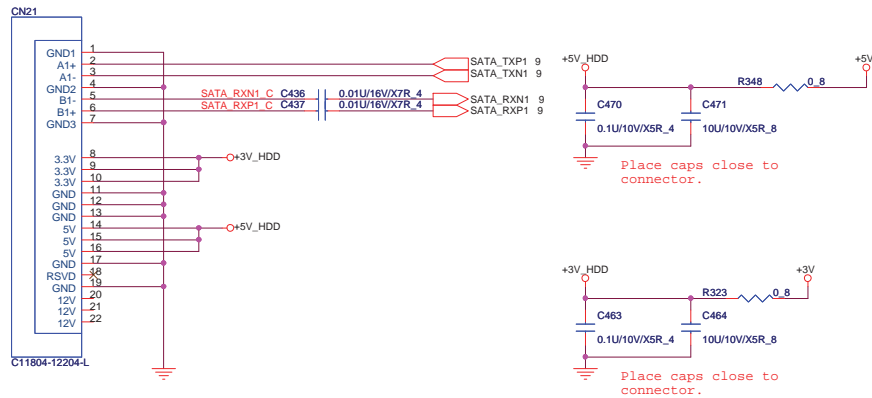
Speaker(AMP)



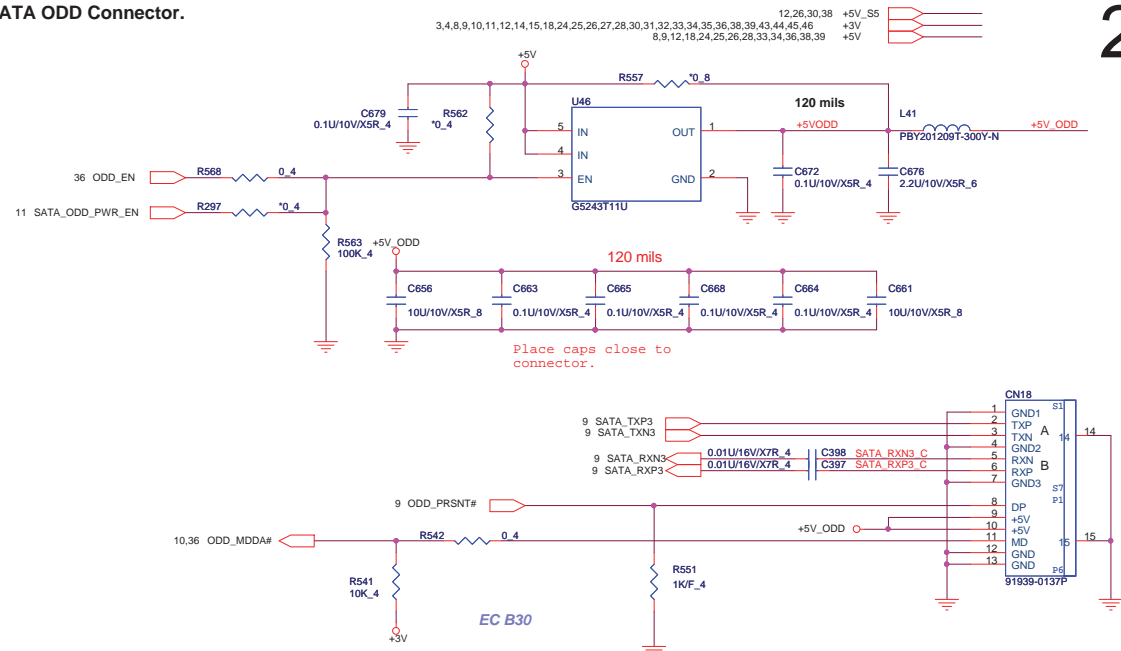
PC BEEP



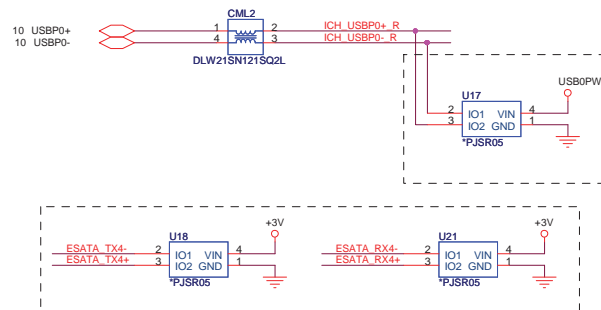
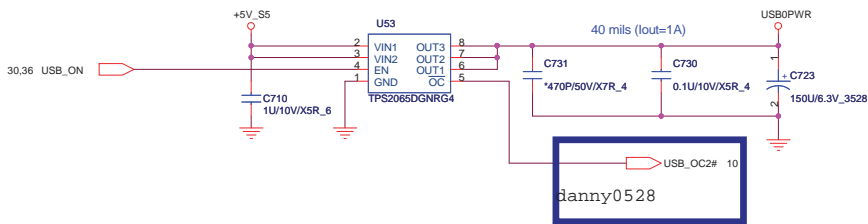
SATA HDD Connector.



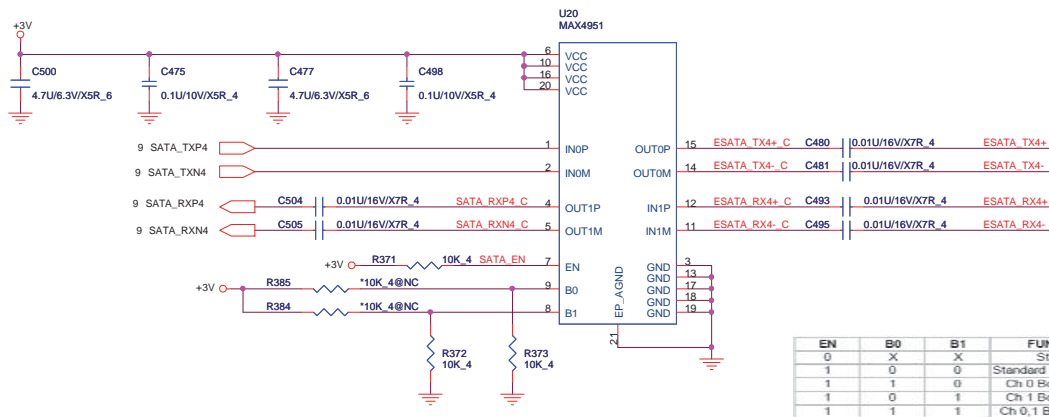
SATA ODD Connector.



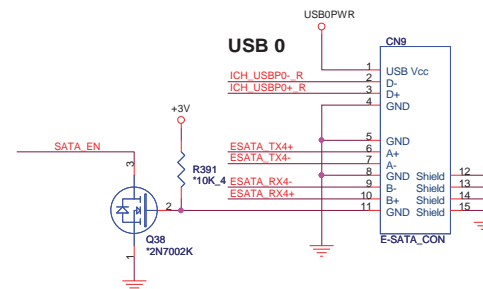
USB + E-SATA



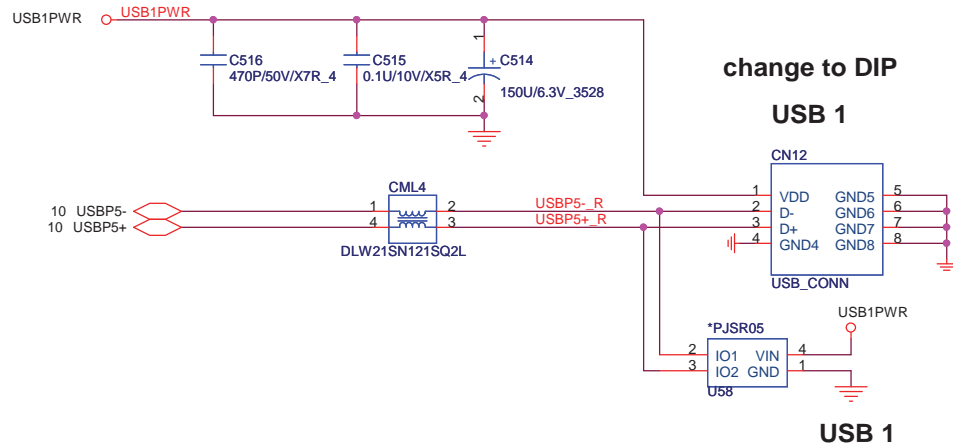
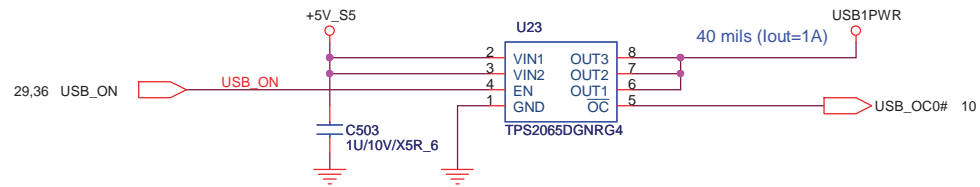
E-SATA RE-DRIVER



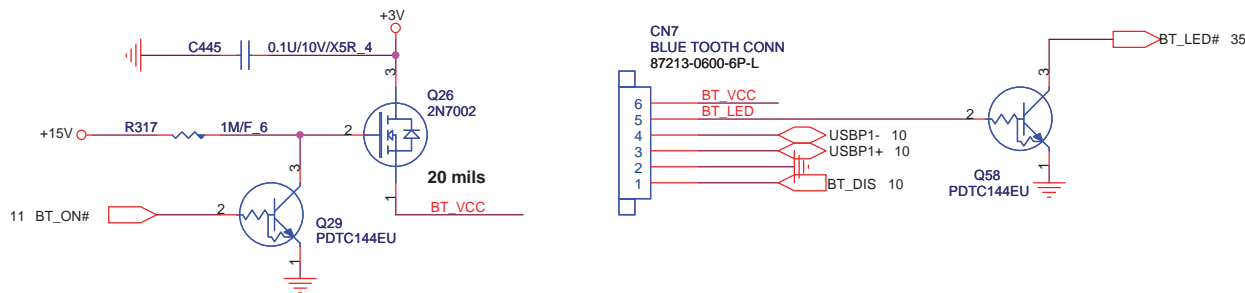
EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0, 1 Boost Output



USBX3

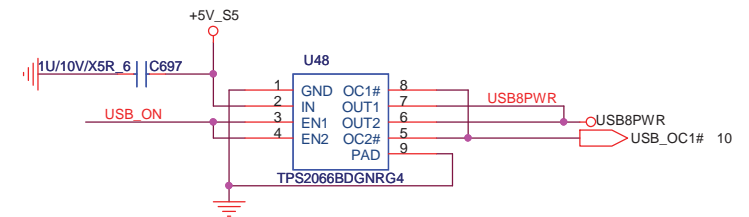
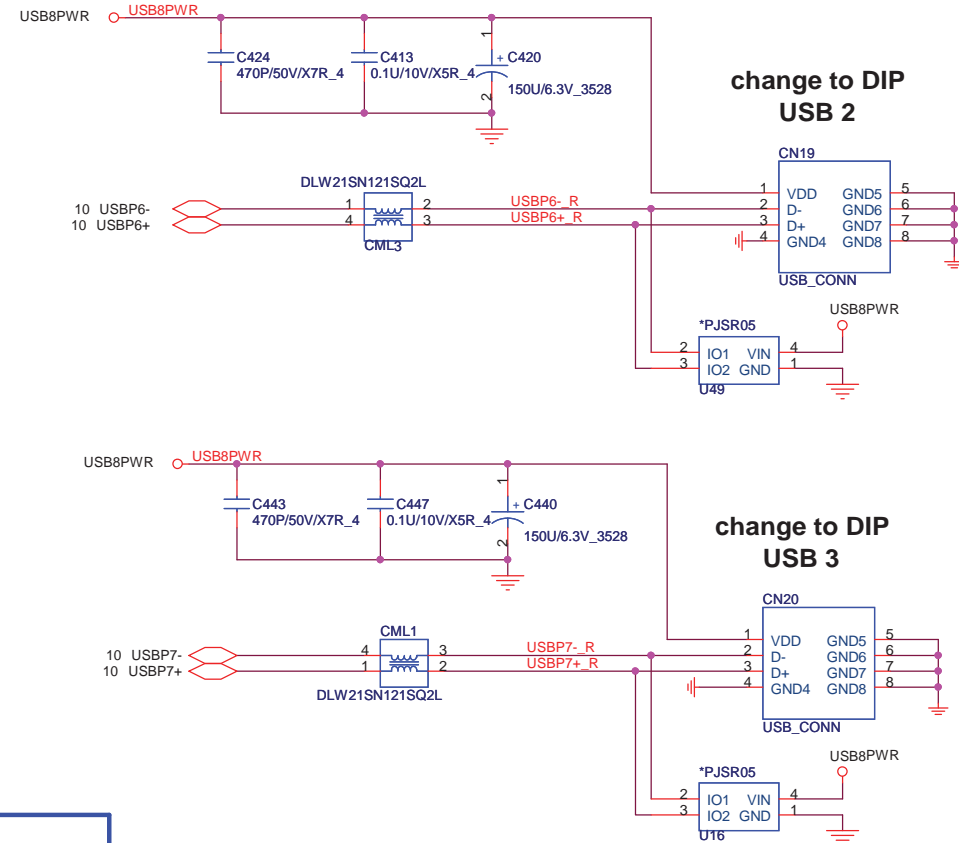


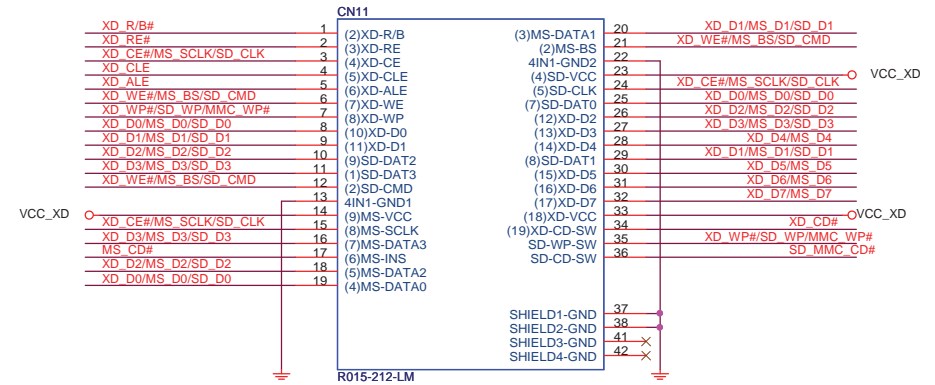
BLUETOOTH



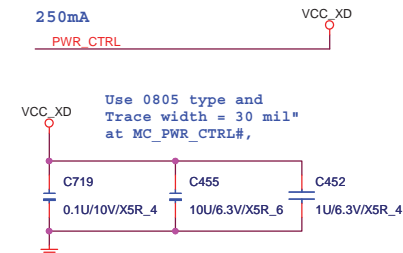
3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,31,32,33,34,35,36,38,39,43,44,45,46
12,26,29,38 +5V_S5
26,28,38,40,42,43 +3V
+15V

29

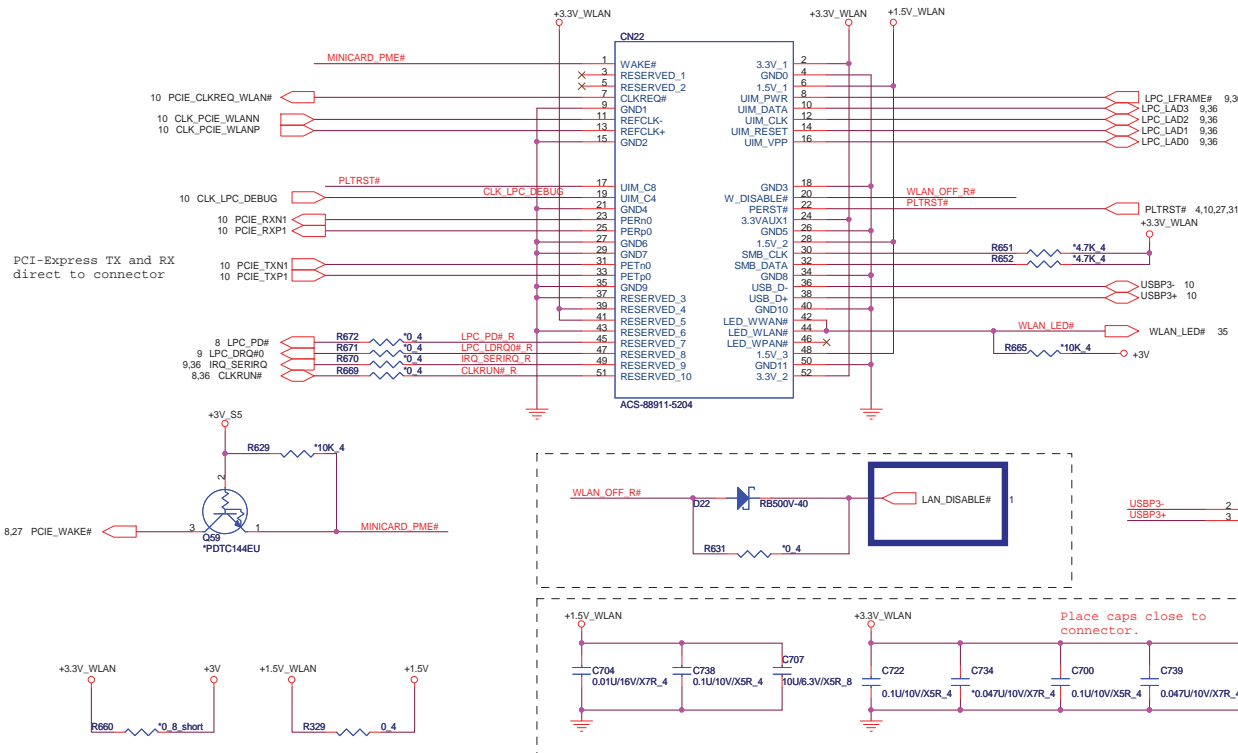
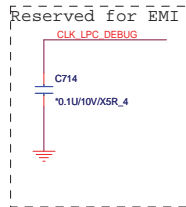




Memory Card Power Supply

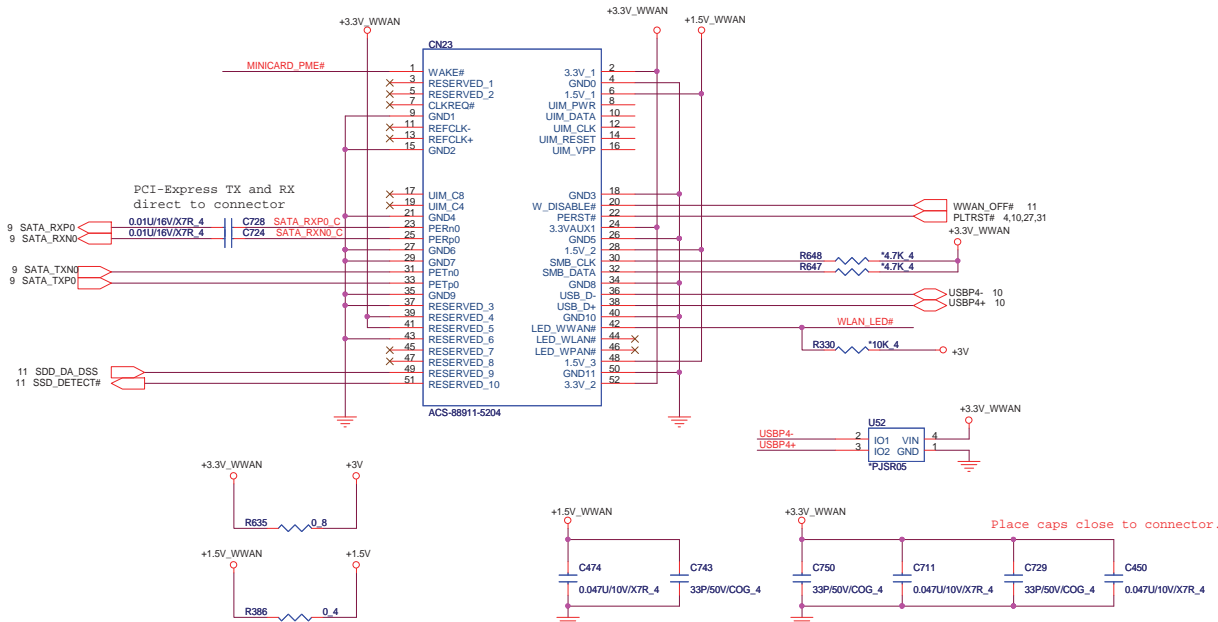


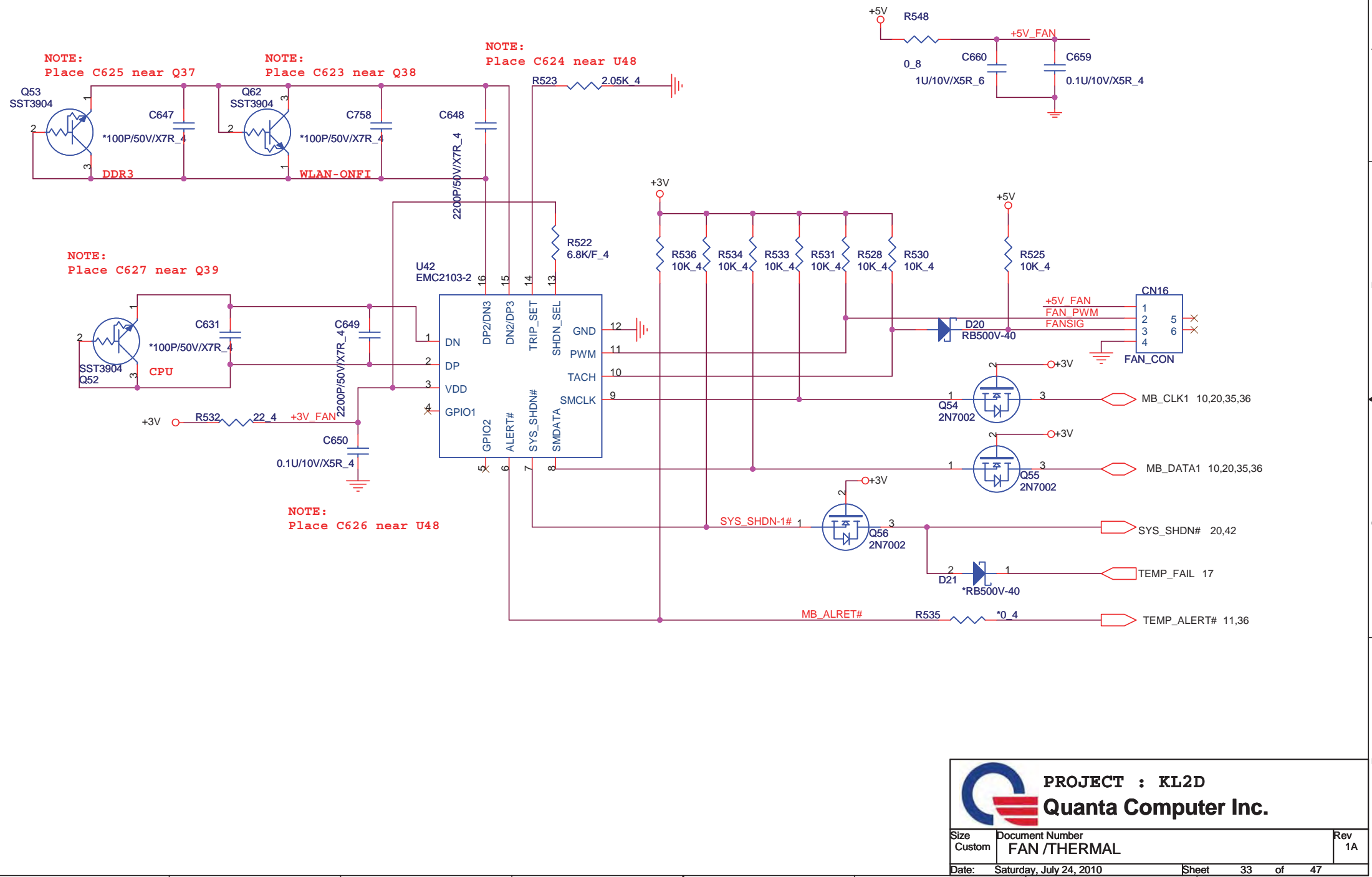
MiniCard WLA connector



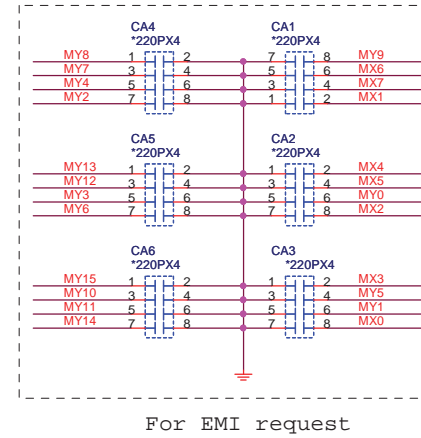
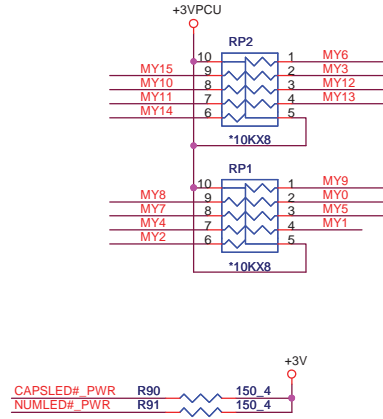
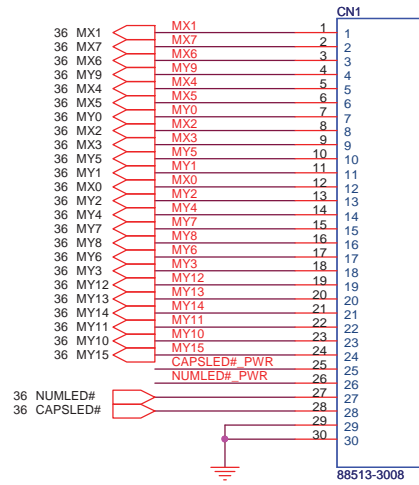
MiniCard WWAN/SATA SSD connector

SIM Card CONN





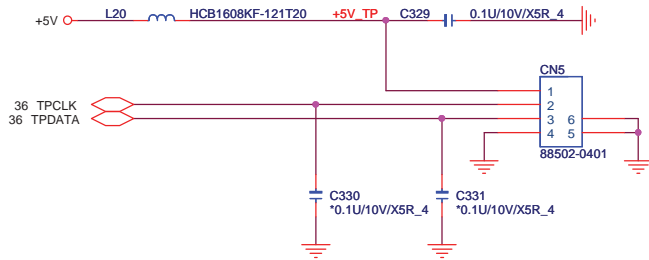
KEYBOARD



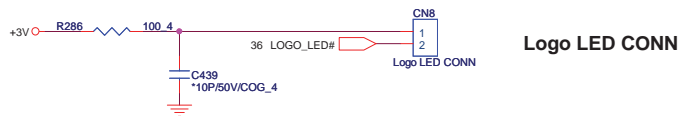
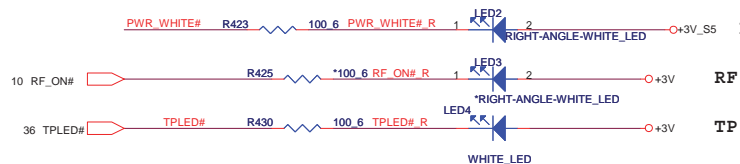
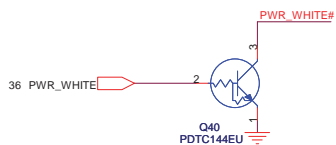
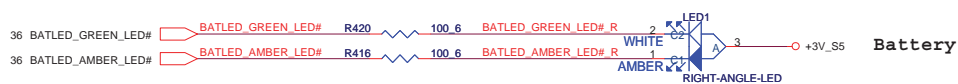
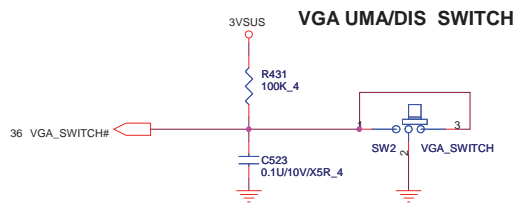
8,9,12,18,24,25,26,28,29,33,36,38,39 +5V
8,9,26,27,35,36,38,39,42,44,46 +3VPCU
26,28,30,38,40,42,43 +15V
3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,31,32,33,35,36,38,39,43,44,45,46 +3V
5VSUS

34

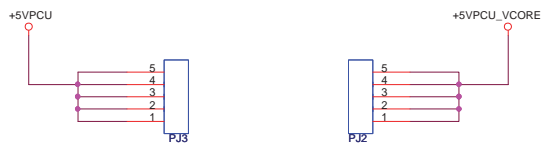
Touch pad



Backlight Keybaord Con.



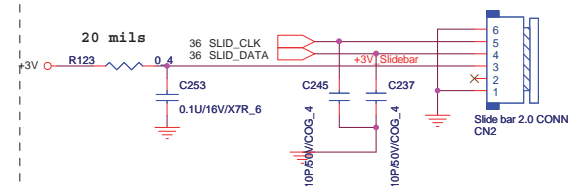
5VPCU Cable for CPU Core Power



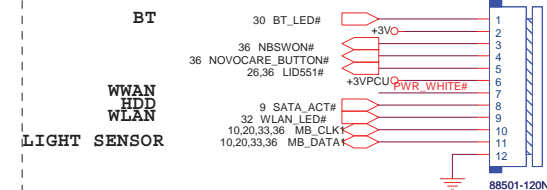
8,9,26,27,34,36,38,39,42,44,46 +3VPCU
3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,31,32,33,34,36,38,39,43,44,45,46 +3V
36,38,44 3VSUS

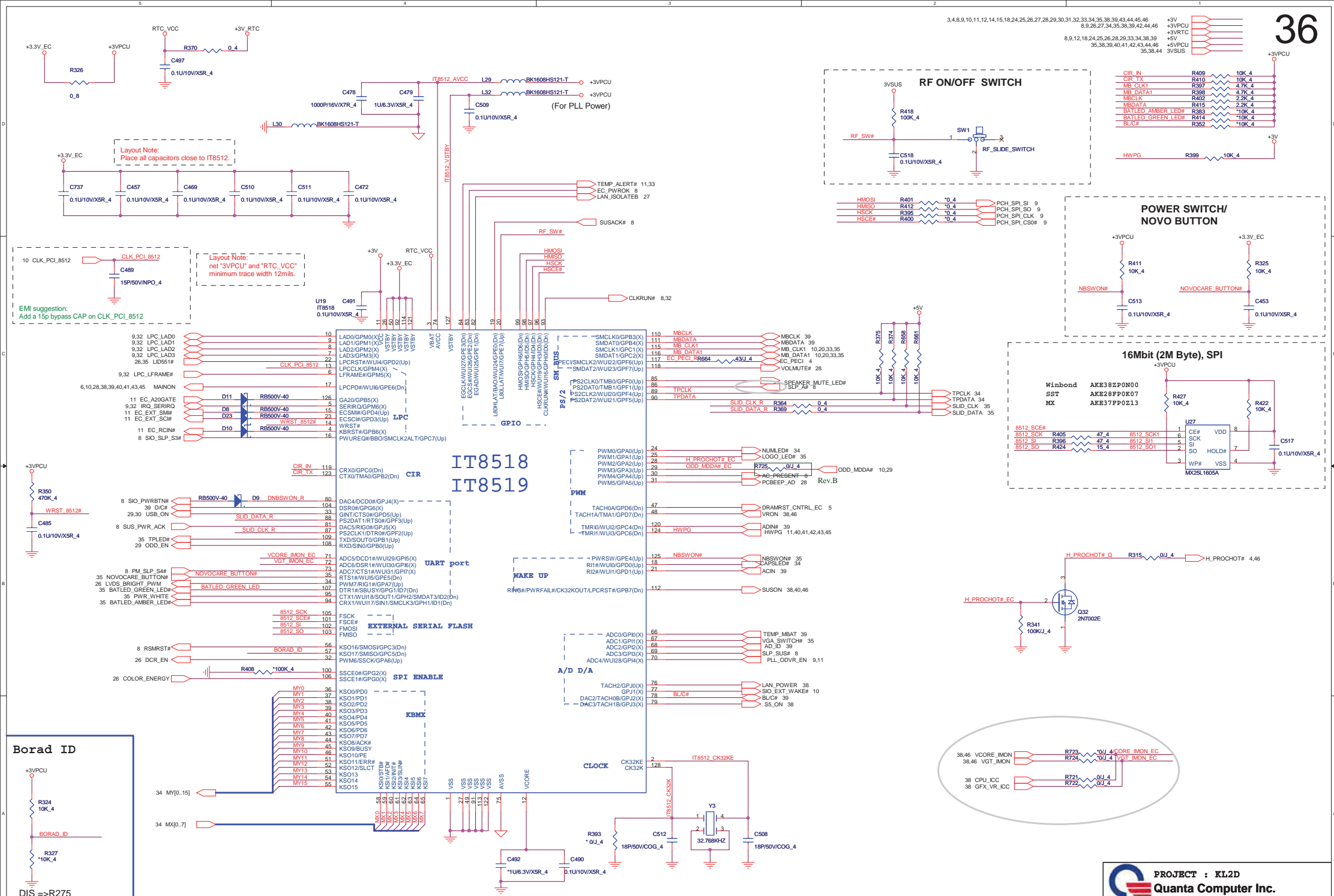
35

Slide bar 2.0

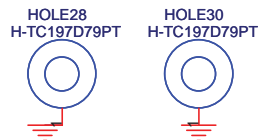


POWER BOARD

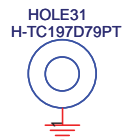




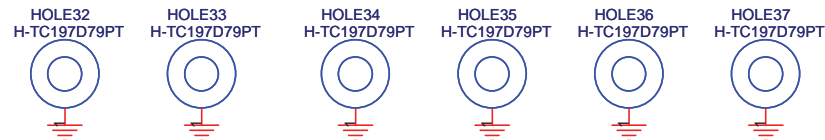
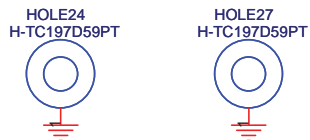
MiniCard WLAN



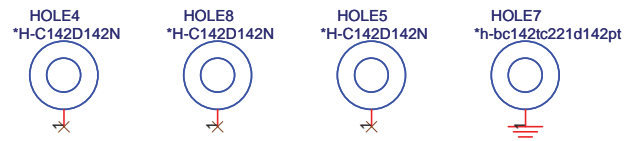
MiniCard WWAN



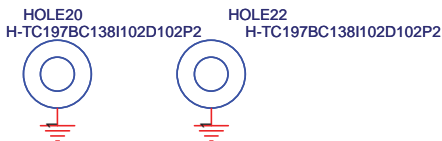
Hole for PCH support



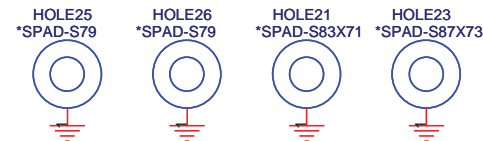
Hole for CPU support



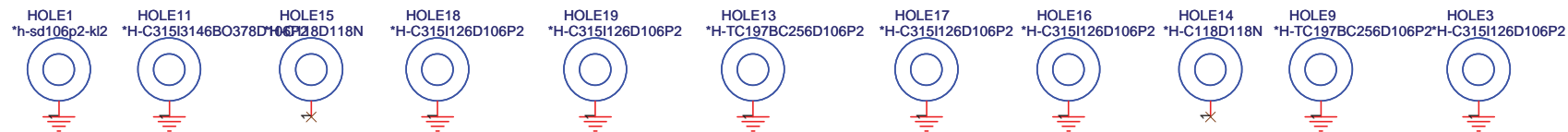
VGA nut



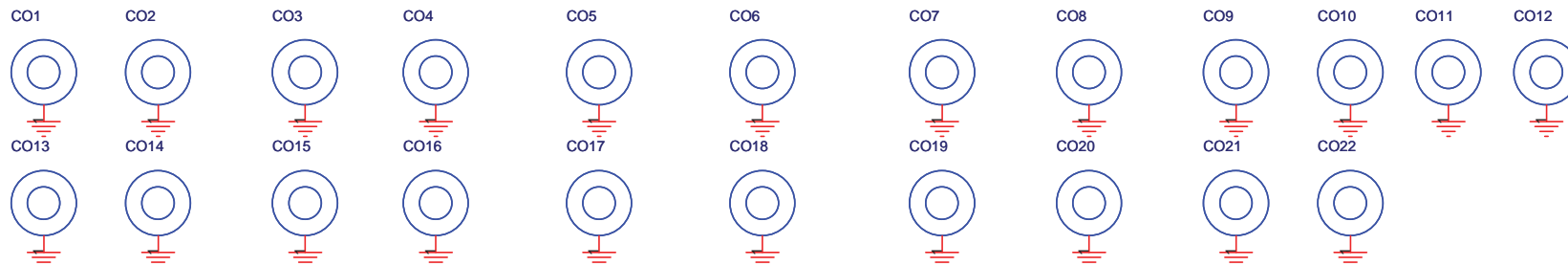
PAD



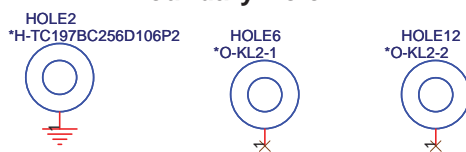
Boundary Hole



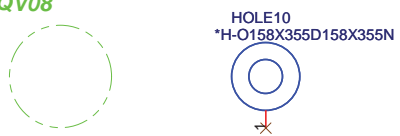
ESD Mask Copper




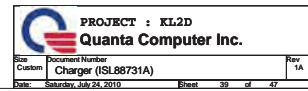
Boundary Hole

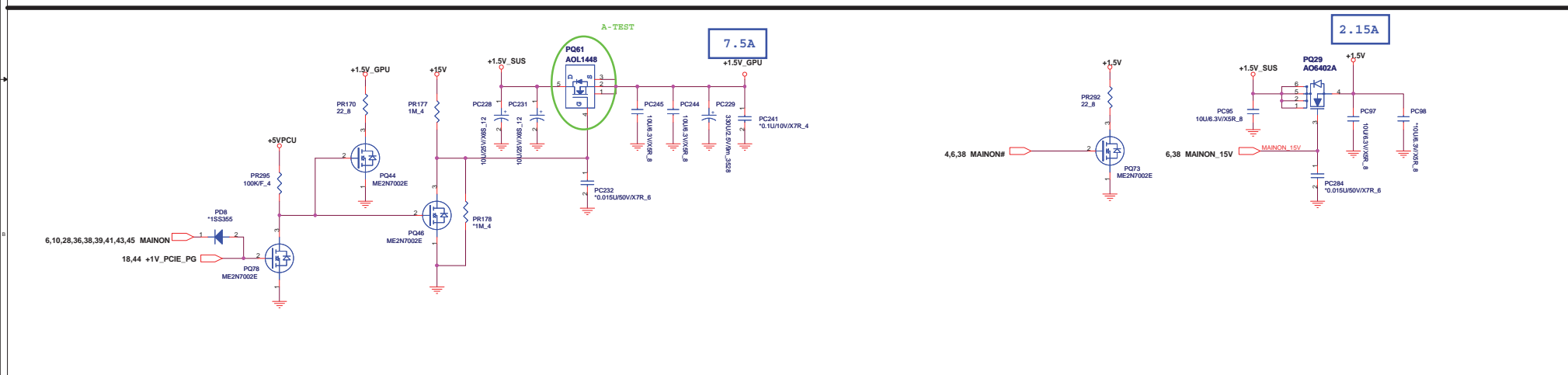
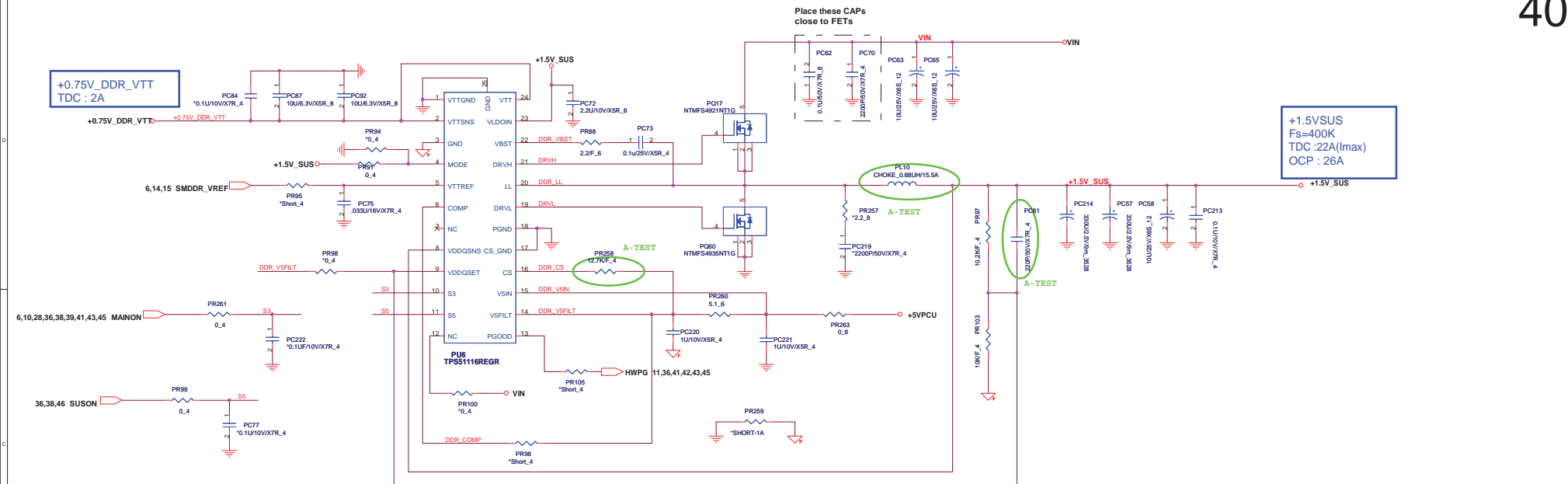


HDD PAD EC QV08

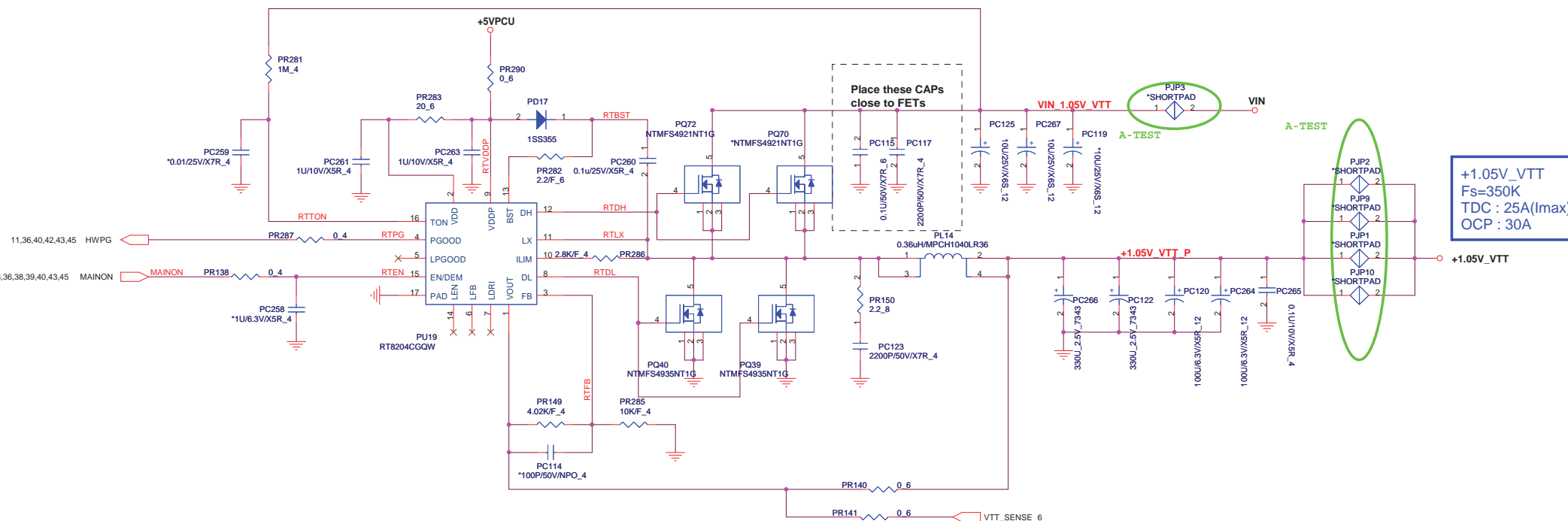


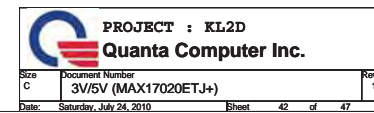
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Date: Saturday, July 24, 2010		
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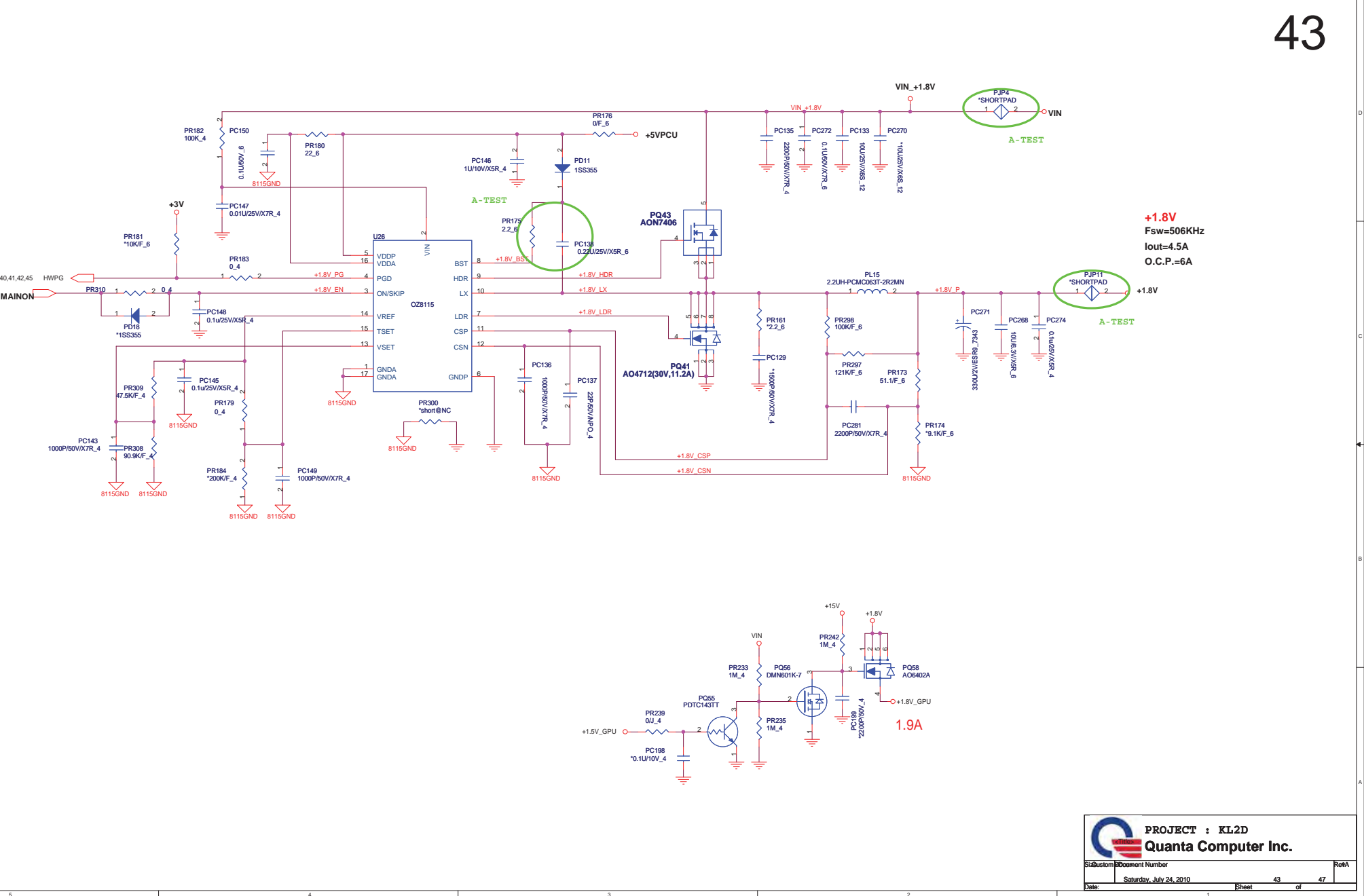


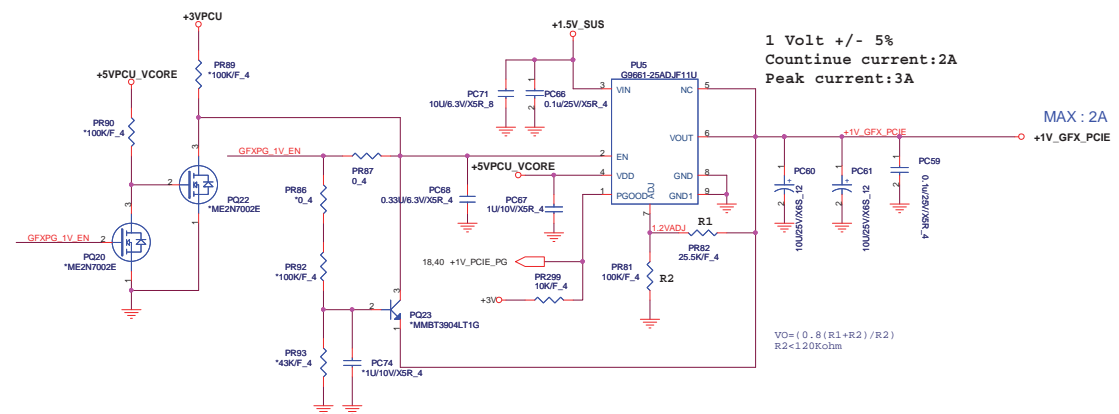
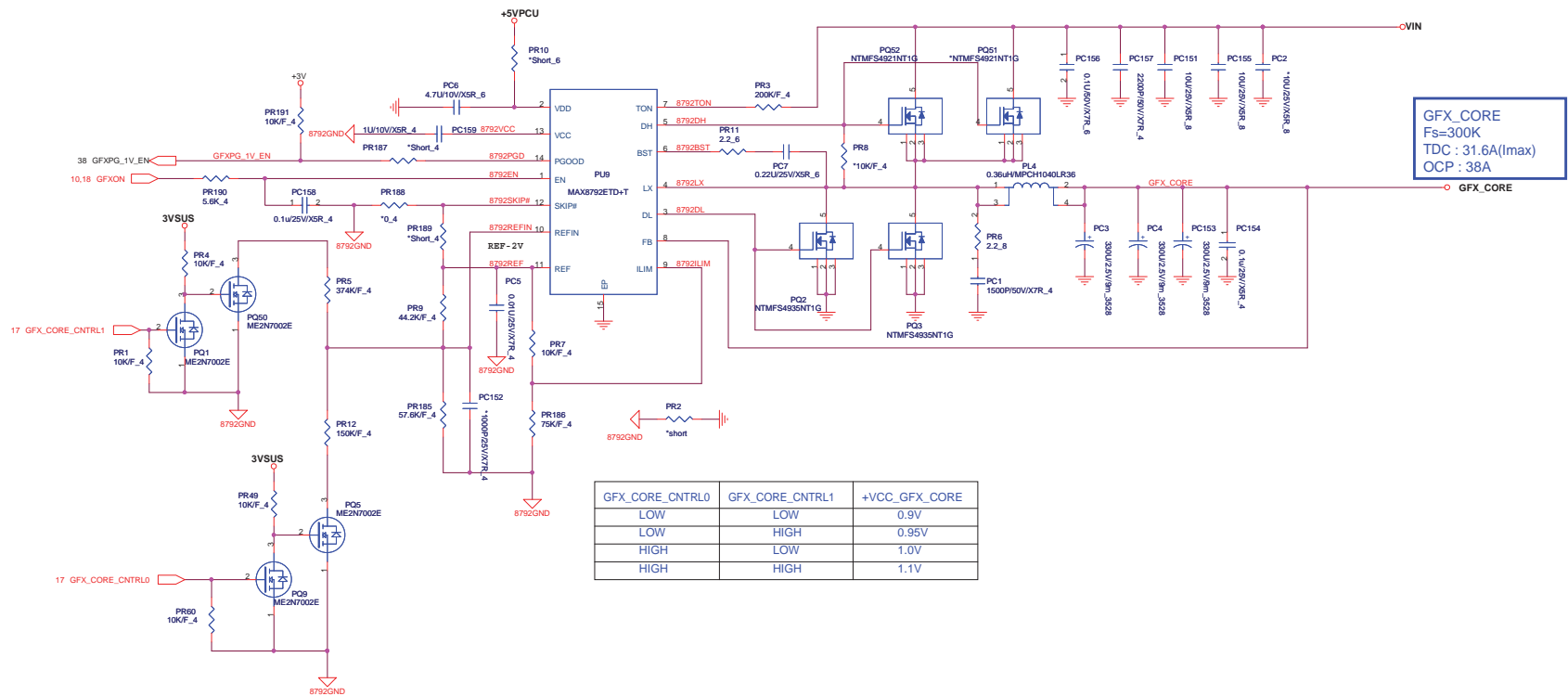


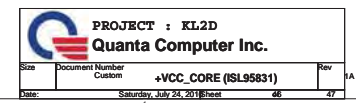
For S3 Power Saving











EC #	Page	Description	Part Affected